# ANALOG PREDISTORTION FOR IMPROVEMENT OF RF POWER AMPLIFIER EFFICIENCY AND LINEARITY

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# ANALOG PREDISTORTION FOR IMPROVEMENT OF RF POWER AMPLIFIER EFFICIENCY AND LINEARITY

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To my family and friends.

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# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| Ω | ohm |
| ° | degree |
| 2G | second generation |
| 3G | third generation |
| 4G | fourth generation |
| ACPR | adjacent channel power ratio |
| ADS | Advanced Design System |
| AM-AM | amplitude-amplitude modulation |
| AM-PM | amplitude-phase modulation |
| dB | decibel |
| dBc | decibel relative to a carrier level |
| dBm | decibel relative to a miliwatt |
| DC | direct current |
| DPD | digital predistortion |
| EVM | error vector magnitude |

| | |
|---|---|
| FB | feedback |
| FF | feedforward |
| GHz | giga hertz |
| Hz | hertz |
| I | in-phase |
| IC | integrated circuit |
| IMD | intermodulation distortion |
| LTE | long term evolution |
| MHz | mega hertz |
| NF | noise figure |
| OFDM | orthogonal frequency-division multiplexing |
| PA | power amplifier |
| PAR | peak-to-average power ratio |
| PC | personal computer |
| PCB | printed circuit board |
| Q | quadrature-phase |
| QAM | quadrature amplitude modulation |

| | |
|---|---|
| QPSK | quadrature phase shift keying |
| RF | radio-frequency |
| SiGe | silicon-germanium |
| SMD | surface mount device |
| SP6T | single-pole six-throw |
| VGA | variable gain amplifier |
| VMOD | vector modulator |
| VPS | variable phase shifter |
| WCDMA | wideband code division multiple access |

# SUMMARY

The objective of this research is to implement analog systems that enable highly efficient and linear operations of the RF PAs used in wireless communication systems. The ever-growing smartphone market and a large number of wireless subscribers have given rise to complex modulation schemes having a high spectral efficiency. One of the drawbacks in the modern wireless waveform is its high PAR. This high PAR requires PAs in RF transmitters to operate with a large output back-off to fulfill linearity specifications, which in turn results in lower power efficiency. To relieve this trade-off between linearity and efficiency, DSP-based techniques such as crest factor reduction (CFR) of the waveforms and PA linearization by digital predistortion (DPD) have been widely investigated and commercialized. However, DSP-based approaches consume significant DC power. Because smaller PAs are more frequently deployed in today's cellular networks, such power consumption can be prohibitive. To cope with these problems, APD techniques have been developed while providing higher levels of performance required by 4G cellular systems in this work.

The critical analog circuits for use in the above analog systems are identified: RF variable gain amplifier (VGA), RF variable phase shifter (VPS) and RF logarithmic amplifier (log amp). Especially, to achieve adequate linearization in an APD system, there are special demands on these analog parts, which are not typical concerns for other applications that may use similar components. Analog circuits are designed, and their performances are experimentally verified in this research.

Finally, an APD system is implemented in board levels by mounting the fabricated analog circuits on printed circuit boards (PCBs). Digital control capabilities are added to this system by calibrating each gain of the limiter stages in the log amp and utilizing digital-to-analog converters (DACs) and digital potentiometers. These capabilities have enabled find the optimal operating points where the performances of the APD system are maximized.

# CHAPTER 1

# INTRODUCTION

## 1.1 Motivation

A radio frequency (RF) power amplifier (PA) is one of the most important components in wireless communication systems because its performance determines many overall system specifications. There are two aspects that PAs in RF transmitters must have: good linearity and high efficiency. Specifically, PAs have to be linear enough to ensure a good quality of transmitted signals from an RF transmitter and be highly efficient to extend the battery life in handset applications.

The exponential growth in wireless subscribers in the last decades has motivated the development of highly spectrum-efficient modulation schemes. As Table 1.1 shows, the wireless technology has evolved in such a way that employs complex digital modulation schemes and multicarrier structures to optimize the use of spectrum or bandwidth. For instance, orthogonal frequency-division multiplexing (OFDM) is a popular modulation scheme in the modern high-speed communication because of its high spectral efficiency achieved by using a large number of parallel narrow-band subcarriers. However, the main drawback of the modern wireless waveform is its high peak-to-average power ratio (PAR). In OFDM systems, signals can have peaks that exceed 12 dB above the average signal power. This high PAR is inevitable since a waveform shows higher peaks as more signals are modulated onto a composite signal.

**Table 1.1** Comparison of wireless technology standards (downlink)

| Technology | Modulation | Carrier Structure | Carrier BW | PAR |
|---|---|---|---|---|
| GSM (2G) | GMSK | Single-Carrier | 0.2 MHz | 0 dB |
| EDGE (2.5G) | 8PSK | Single-Carrier | 0.2 MHz | 3.2 dB |
| WCDMA (3G) | QPSK | WCDMA | 5 MHz | 3.5 – 7 dB |
| LTE (4G) | QPSK, 16QAM, 64QAM | OFDM | 1.5 – 20 MHz | 10 -12 dB |

Efficiency in PAs is highest when they are operated near a saturation region, but this inherently leads to signal distortions [1, 2]. A simple method to maintain linearity is to operate PAs at a lower average power level. This technique is called "back-off." Higher PAR of waveforms requires PAs in RF transmitters to operate with a larger output back-off to avoid PA saturation and maintain linearity at high output power. This backed-off mode leads to poor power efficiency in PAs and the transmitters. The trade-off between the efficiency and the linearity is the one of the most critical design considerations for RF PA designers. To relieve this performance degradation, various techniques that simultaneously achieve high efficiency and good linearity have been investigated and proposed. Two popular techniques among them are PAR reduction and PA linearization.

PAR reduction (also known as crest factor reduction or CFR) is a technique often employed to modify waveforms to enable PAs to operate at higher output average power and achieve higher efficiency [3, 4]. It is well known that a simple clipping generates excessive in-band and out-of-band interferences [5, 6]. Many PAR reduction techniques have been developed such as companding, coding, tone reservation, tone injection, active constellation extension, partial transmit sequence, selected mapping, and constrained clipping [3]. These PAR techniques have one thing in common, which is that they utilize

digital signal processing (DSP) to shape out waveforms deliberately to reduce PAR without spectral regrowth or spectrum distortions.

There are linearization techniques that allow a more efficient use of PAs by compensating the nonlinear distortion produced by PAs. Especially, digital predistortion (DPD), initially reported in 1983 [7, 8], has been widely investigated and has become one of the most fundamental building blocks in a modern wireless communication system. DPD has been more popular and showed superior performance when compared to analog predistortion (APD) because a DSP is faster, more accurate, and more flexible in handling data than analog signal processing.

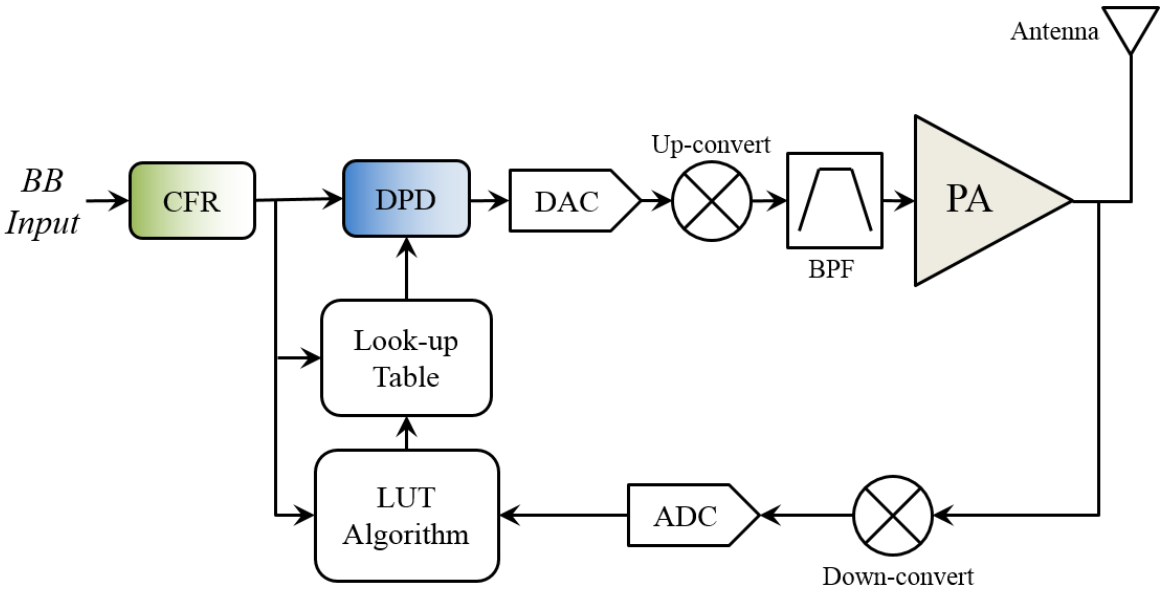



**Figure 1.1** Typical modern transmitter including CFR and DPD

As explained above, DSP-based approaches have been popular for use in macro-cell base stations over the last decade. Figure 1.1 shows the typical transmitter used today's

cellular network, which includes CFR and DPD technologies [9, 10]. However, DSP-based approaches consume significant DC power. Because macro-cells, which are also known as towers, struggle to penetrate the innards of building, small cells such as micro-cells, pico-cells, and femto-cells are used to enhance indoor coverage. Therefore, smaller PAs are more frequently being deployed in today's cellular networks. As the sizes of cellular base stations and PAs get smaller, their output power ranges also decrease, as shown in Table 1.2. Therefore, the high power consumption of DSP-based PAR reduction or PA linearization techniques can be prohibitive for use in small-cell base stations and mobile phones.

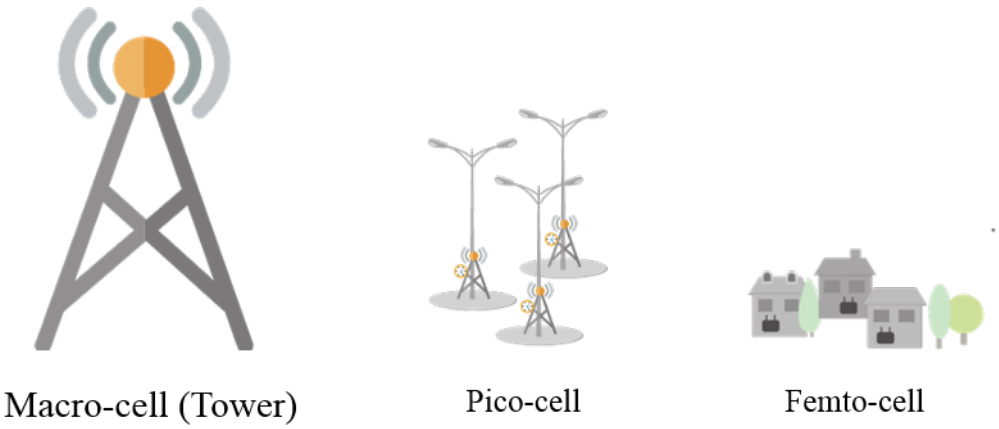



**Figure 1.2** Small-cell base stations

**Table 1.2** Output RF power comparison between various sizes of base stations

| | **Macro** | **Micro** | **Pico** | **Femto** |
|---|---|---|---|---|
| Max Pout | 50 dBm | 38 dBm | 30 dBm | 24 dBm |

Analog signal processing techniques cannot outperform DSP-based techniques due to their limited dynamic range and accuracy of analog components. If such analog approaches can provide adequate performances, then they may become attractive solutions for use in the small (nano, pico, etc) base stations due to their lower complexity, lower power consumption, and compact size.

This work presents an analog system that helps PAs operate at high efficiency and have good linearity simultaneously.

## 1.2 Thesis Organization

The goal of this dissertation is to illustrate the feasibility of an analog system that helps PAs to operate at high efficiency and have a good linearity, simultaneously. DSP-based approaches, used to improve the performance of PAs, show limitations for applications, such as small cell base stations or mobile phones. The research presented here will identify the limitations of previous analog linearization techniques and will demonstrate a new analog method to address those constraints.

In Chapter 2, the origin of PA problems and the history of resolving them are addressed. The reader will be introduced to state-of-the-art analog predistortion techniques that were published and proposed for the last decades. The advantages and shortcomings of such an implementation are highlighted.

The important analog components for use as an RF predistorter in APD predistortion systems are identified and characterized through computer simulations in Chapter 3. Specifically, a variable phase shifter (VPS) as a phase predistorter in the APD, and a variable gain amplifier (VGA) as an amplitude predistorter for use in the APD applications will be presented. These two circuits were integrated and fabricated into one

die. This chapter shows how the RF predistorters are designed and measured results got from the fabricated circuits

Chapter 4 presents a logarithmic amplifier (log amp) design for use as an RF power detector in APD systems. First of all, this chapter goes through the required specifications that the log amp in the APD systems needs to detect AM-AM errors of an RF PA. The log amp presented in this chapter operates fast with less than 2.2 ns response time by employing the fast rectifier having a compound PNP and NMOS. Also, this log amp is digitally calibratable by adding current DACs to each limiter stage. The log amp has been fabricated using a SiGe BiCMOS 0.18-um process and verified experimentally.

The analog predistortion system that uses the analog circuits developed in Chapter 3 and 4 is described in Chapter 5. The log amp and a phase detector are used to estimate the AM-AM and AM-PM errors of PAs respectively. The outputs of the log amp and phase detector control the VGA and VPS to correct the errors of PAs. By employing the fast and accurate analog circuits as well as digital calibrating capabilities, the APD system achieves a 5 dB ACPR correction with an LTE 10 MHz signal. This chapter will address the limitations of the APD systems from the measured results.

Finally, Chapter 6 summarizes and concludes the work in this dissertation.

# CHAPTER 2

# ORIGIN AND HISTORY OF PROBLEM

## 2.1 Introduction

Power amplifiers (PAs) in RF transmitters increase the power of RF signal so that RF receivers can sense this signal. The output of a PA feeds an antenna that broadcasts the signal into the air. As Figure 2.1 shows, a PA is the most power-hungry block in an RF transceiver, and thus, its efficiency determines the overall efficiency of an RF transceiver. Since a PA with a higher efficiency converts a given power supply into more useful power and produces less heat than one with a lower efficiency, additional cost savings are expected in the power supply and cooling by improving PA efficiency.

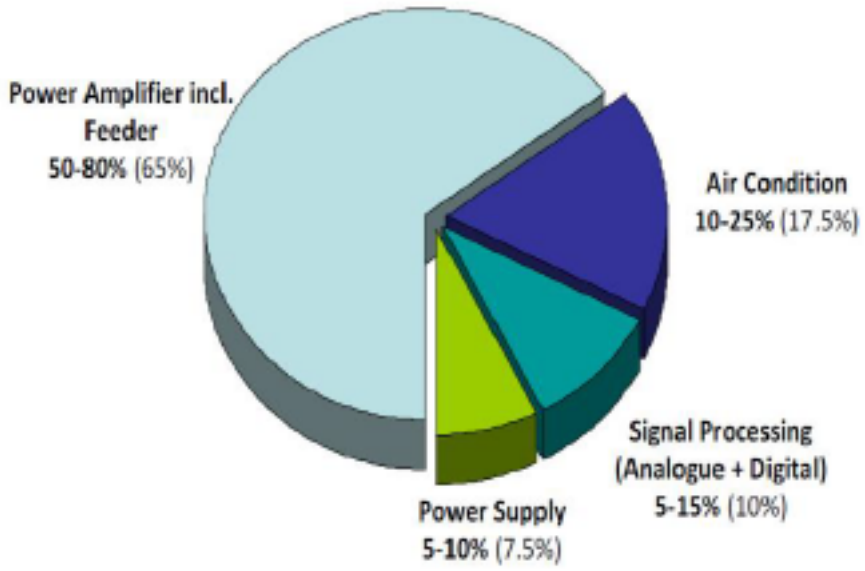



**Figure 2.1** Breakdown in power consumptions in radio base station [11]

For a given supply power, a PA that feeds a higher power to an antenna achieves a higher efficiency in a PA. However, the desired linearity performance is obtained by decreasing an output power level from the maximum power level that a PA can produce. The linearization of PAs reduces this amount of back-off, thus increasing the efficiency in PAs as well as RF transmitters. So, understanding the behavior of PAs is important when applying linearization techniques to PAs.

In this chapter, nonlinear behaviors and memory effects of PAs are described. Also, the history of efforts to solve the problems that PAs have had over the past decades have will be presented and explored.

## 2.2 Memoryless PA Behavior Modeling

As illustrated in Figure 2.2, a PA can be drawn with one block in the system level considering $x$ as an input signal and $y$ as an output signal.

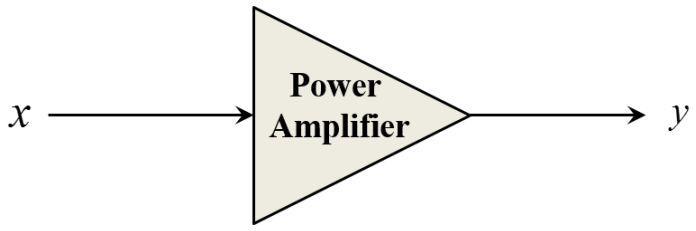



**Figure 2.2** Power amplifier input-output diagram

In a linear system having the transfer function of $T(x)$, the output of this linear system becomes $c_1 \cdot T(x_1) + c_2 \cdot T(x_2)$ for the input $c_1 \cdot x_1 + c_2 \cdot x_2$. Unfortunately, a PA is a nonlinear system and generates a large number of additional terms at different

frequencies from the input signal. The nonlinear effects of memoryless PAs are often modeled with the polynomial expression, which is written as (2.1). The coefficient $a_0 - a_3$ are complex values.

$$y = a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 \tag{2.1}$$

Memory effects refer to the changes in the amplitude and phase of distortion components caused by changes in modulation frequency [12]. The simple modeling using a polynomial expression such as (2.1) does not include memory effects of PAs, but understanding memory effects of PAs play critical roles in maximizing the effect of PA linearization techniques. These memory effects will be further discussed later in this chapter.

A useful method to characterize a memoryless system is to apply two closely spaced fundamental signal tons to a test amplifier. Assume that two signals with same amplitude $A$ at different frequencies $w_1$ and $w_2$ as shown in (2.2) are applied to the polynomial model in (2.1).

$$x(t) = A\cos w_1 t + A\cos w_2 t \tag{2.2}$$

From (2.1) and (2.2), the output of the PA model can be described as (2.3). As shown in (2.3), the output signal of a PA includes not only fundamental tones but also harmonics and intermodulation products.

$$
\begin{aligned}
y(t) &= a_0 + a_1 A x(t) + a_2 A^2 x^2(t) + a_3 A^3 x^3(t) \\
&= (a_0 + a_2 A^2) + \left(a_1 A + \frac{9}{4} a_3 A^3\right)(\cos w_1 t + \cos w_2 t) \\
&\quad + a_2 A^2 \{\cos(w_1 + w_2)t + \cos(w_2 - w_1)\} \\
&\quad + \frac{a_2 A^2}{2}(\cos 2w_1 t + \cos 2w_2 t) \\
&\quad + \frac{3a_3 A^3}{4}\{\cos(2w_1 + w_2)t + \cos(2w_2 + w_1)t + \cos(2w_1 - w_2)t \\
&\quad + \cos(2w_2 - w_1)\, t\} + \frac{a_3 A^3}{4}(\cos 3w_1 t + \cos 3w_2 t)
\end{aligned}
\tag{2.3}
$$

The output of the PA model, $y(t)$, can be illustrated in frequency domain, as depicted in Figure 2.3. The third-order intermodulation products at $2w_1 - w_2, 2w_2 - w_1$ are quite close to fundamental tones, so that they are hard to eliminate by a band-pass filter. Amplitude of third-order intermodulation (IM3) can be written as (2.4).

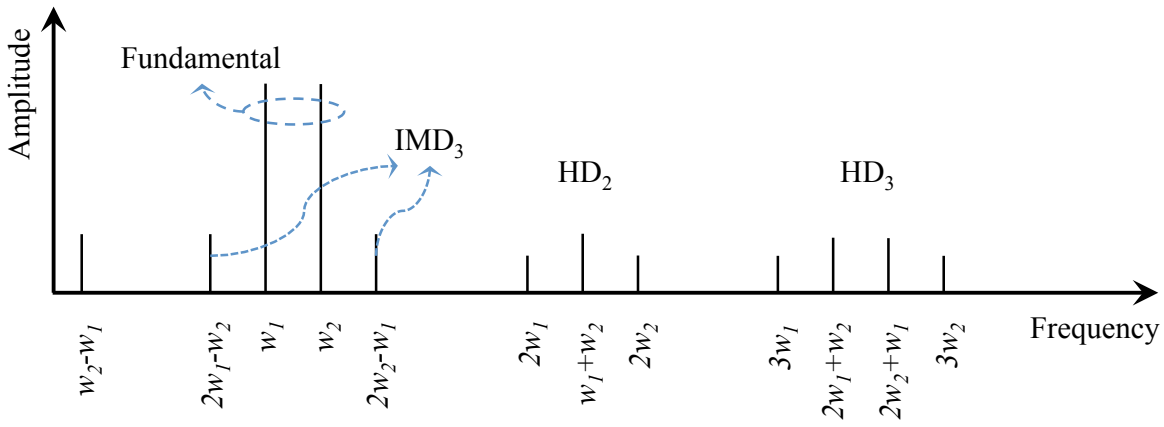



**Figure 2.3** Frequency spectrum of the PA output

$$IM3 = \frac{3}{4} \cdot a_3 \cdot A^3 \tag{2.4}$$

The IM3 increase by 3 dB for every 1 dB increase in fundamental tones. Therefore, the amplitude of $\mathrm{x(t)}$ increases, the amplitude of IM3 increases sharply and, at some point, becomes equal to that of the fundamental tones at the output. Input-referred third intercept point, $\mathrm{IIP_3}$, is the metric that indicates the input power level at which amplitude of the IM3 and fundamentals tone becomes equal at the output. These amplitudes can be equated, as shown in (2.5) to derive the $\mathrm{IIP_3}$.

$$\mathrm{a_1 A} = \frac{3\mathrm{a_3 A^3}}{4} \tag{2.5}$$

$$A_{IIP3} = \sqrt{\frac{4|a_1|}{3|a_3|}} \tag{2.6}$$

Usually, other harmonics and intermodulation products do not draw attention because band-pass filters can easily eliminate them. However, in (2.3), fundamental tones include nonlinear term, $\frac{9}{4}a_3A^3$, which causes in-band distortions. Usually, the coefficient, $a_3$, of polynomial expressions of a PA model is negative value. This nonlinear term in fundamental tones explains a gain compression that occurs when the input power of a PA is increased to a certain level. Interestingly, there is a common rule of thumb for the relationship between the IP3 and the 1dB compression point (P1dB).

$$\frac{A_{IIP3}}{A_{P1dB}} \approx 10\sim12\ dB \tag{2.7}$$

## 2.3 Characterizations of a PA with a Small Memory (Quasi-memoryless PA)

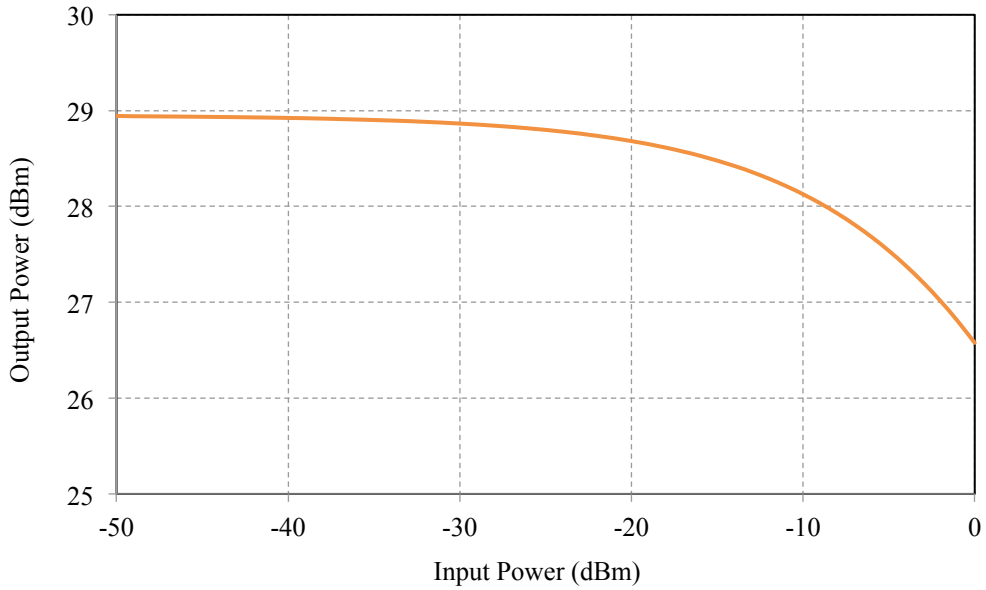
In general, a nonlinear memoryless system only has an amplitude distortion, not a phase distortion [13]. A PA with a small memory is considered as a quasi-memoryless PA system, showing a phase distortion as well as an amplitude distortion. The nonlinear polynomial model specified in (2.3) is adequate for determining amplitude distortions in a PA, but not for phase distortions. Quasi-memoryless systems can be modeled by an amplitude-amplitude (AM-AM) components and an amplitude-phase (AM-PM) component. An AM-AM conversion is the measure of amplitude distortions (AM) and an AM-PM conversion is the measure of phase distortions (PM) caused by amplitude variations (AM) inherent in systems. For the modulated input signal $x(t)$ in (2.5), the corresponding output expression of PAs becomes as (2.6).

$$x(t) = A(t)\cos\{\omega t + \emptyset(t)\} \tag{2.5}$$

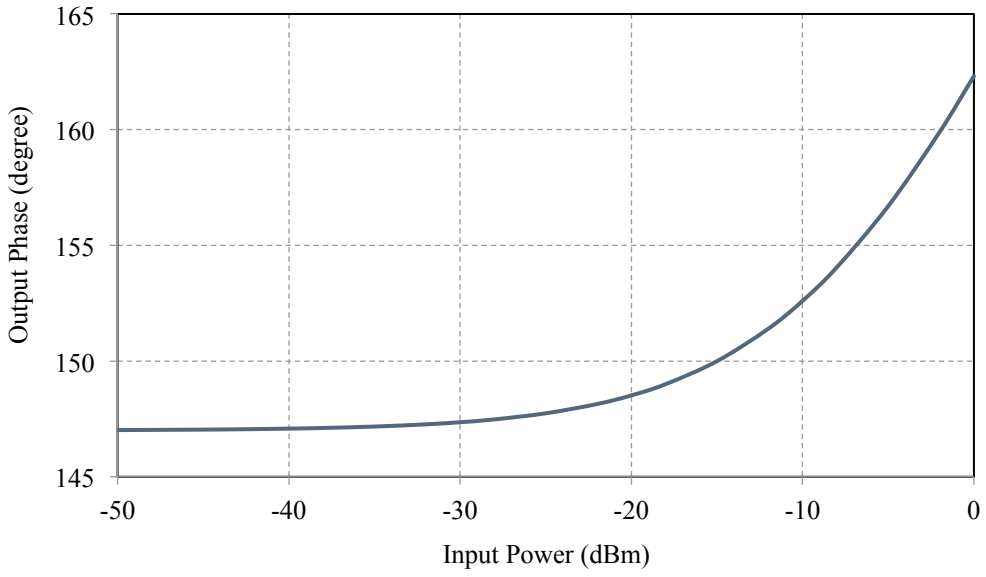
$$y(t) = g\{A(t)\}\cos[\omega t + \emptyset(t) + \psi\{A(t)\}] \tag{2.6}$$

In (2.6), $g\{A(t)\}$ is an AM-AM distortion and $\psi\{A(t)\}$ is an AM-PM distortion. In this system, amplitude and phase distortion depends only on the input signal power.

Figure 2.4 shows an example of AM-AM and AM-PM characteristics of a PA. It was measured by recording a magnitude and a phase of PA gain while sweeping the power of input signal from -50 dBm to 0 dBm. With this behavioral model based on Figure 2.4, system level simulations can be run to see the effects of nonlinearity on modulated RF waveforms.




(a)

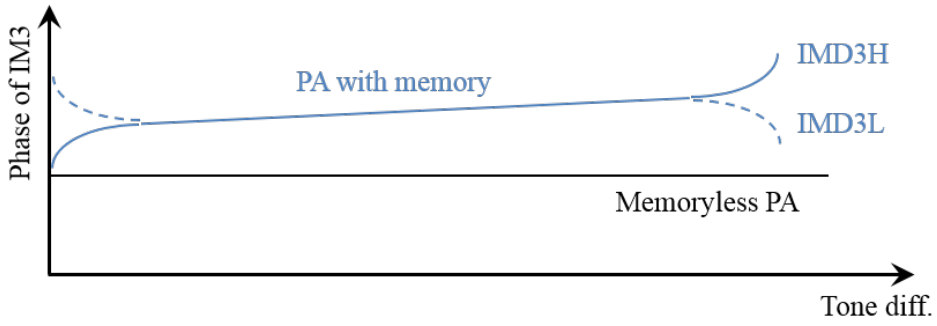



(b)

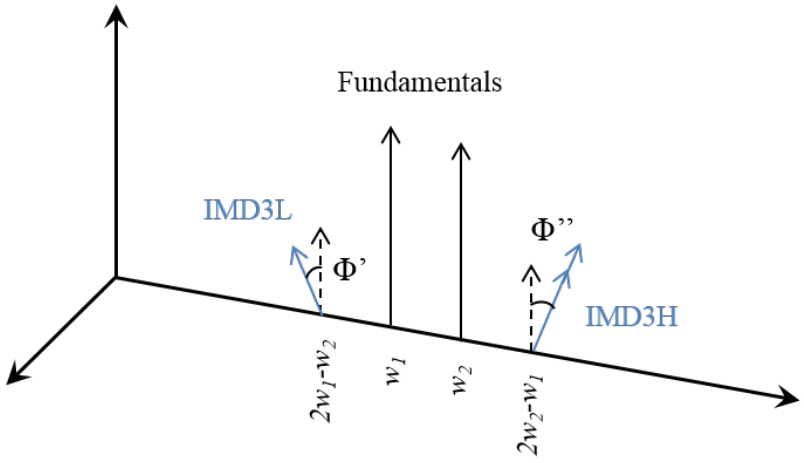
**Figure 2.4** Typical PA nonlinearities (a) Memoryless AM-AM characteristics (b) Memoryless AM-PM characteristic

## 2.4 Memory Effects in PAs

In general, PA systems with small memory effects can be modeled only by AM-AM conversion and AM-PM conversion. For a PA with a large memory, however, the AM-AM and the AM-PM characteristics do not contain complete information of a PA and reduce the accuracy of predistortion models using these characteristics [13]. Memory effects in PAs are the main reason for a memoryless predistorter to have a limited linearization performance.




(a)




(b)

**Figure 2.5** PA memory effects: (a) The phase of IMD products as a function of RF tone spacing (b) The spectral representation of the memory effects using two –tone signal

Also, according to the expressions of IM3 products derived in (2.3), both lower sideband and upper sideband of IM3 have the same amplitude and same phase information to each other, and it is not a function of envelope frequency in memoryless PAs as the shown black line in Figure 2.5 (a). However, the memory effects in RF PAs make IM3 sidebands as a function of tone spacing, and the lower and upper IM3 component could have different relative magnitudes and phases. These phenomena are illustrated in Figure 2.5 (b).

Memory effects in RF PAs arise from many different sources, but the main causes of these memory effects are thermal feedback and bias circuits, which response to the envelope frequencies of modulation signal [12, 14-16]. The reason why the polynomial expressions in (2.3) and (2.6) are insufficient for modeling PAs with memory is that it neglects the cascaded nonlinearity generating mechanisms. To gain insight into the distortion mechanism, let's assume that two-tone RF signal is applied to a PA, and the nonlinearity of which is generated only up to two cascaded stages (highly simplified). In the first stage, a PA will generate distortions including the IM3 calculated from (2.3), and the harmonic tones at various frequencies of $2w_1$, $2w_2$, and $w_2 - w_1$, as shown in Figure 2.3. In the second stage, these generated tones from the two-tone signal will again be mixed to generate IM3 components. For examples, the envelope signal ($w_2 - w_1$) and the upper two-tone signal ($w_2$) are mixed through second-order nonlinearity. Likewise, IM3 components can be created by second order harmonic components ($2w_1$) and RF input tone ($w_2$). As a result, IM3 sidebands are affected not only by fundamental tones but also by tones at the envelope frequencies and other harmonics.

Node impedances of devices such as transistors, biasing and matching network vary over the input signal bandwidth around the carrier frequency and its harmonics, as well as at envelope frequencies. These impedance variations and the cascaded distortion mechanism cause the memory effect, which is called electrical memory effect. However, with careful designs in bias and matching networks, these electrical memory effects are somewhat controllable. Typically, wideband signals (WCDMA, LTE, LTE-A, and etc.) are more sensitive to electrical memory effects.

On the other hands, electro-thermal memory effects are caused by dynamic temperature variations at the devices and components in circuits. In other words, temperature-dependent electrical parameters in devices or components vary their dynamic gains, which typically result in long-time memory effects (>1 μs). Unlikely electrical memory effects, thermal memory effects are unavoidable in most PAs. Narrow-band signals such as EDGE and GSM are more sensitive to electro-thermal memory effects.

## 2.5 Power Amplifier Performance-evaluating Metrics

### 2.5.1 Efficiency

The efficiency of PA is an index that how much DC power is converted to RF output power. The following (2.7) describes PA efficiency. $P_{out}$ is the output power of PA, and $P_{supply}$ is the average power drawn from the supply voltage. Power-added efficiency (PAE) is another metric of rating PA efficiency, which is calculated as (2.8). G in (2.8) is the gain of a PA. When the gain of a PA is sufficiently high, then (2.7) and (2.8) becomes very similar value because $P_{out} - P_{in} \approx P_{out}$.

$$\eta = \frac{P_{out}}{P_{supply}} \tag{2.8}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{supply}} = \frac{P_{out} - P_{out}/G}{P_{supply}} = \eta\left(1 - \frac{1}{G}\right) \tag{2.9}$$

*2.5.2 Adjacent Channel Power Ratio (ACPR)*

PA nonlinearities lead to both an in-band distortion and an out-of-band distortion. $P_{1dB}$, which is measured by using a single-tone signal, and IP3, which is acquired by using a two-tone signal, are not adequate for metrics of PA nonlinearities because modern RF waveforms are digitally- modulated signals that use complex modulations and have different signal statistics from single-tone or two-tone signals.

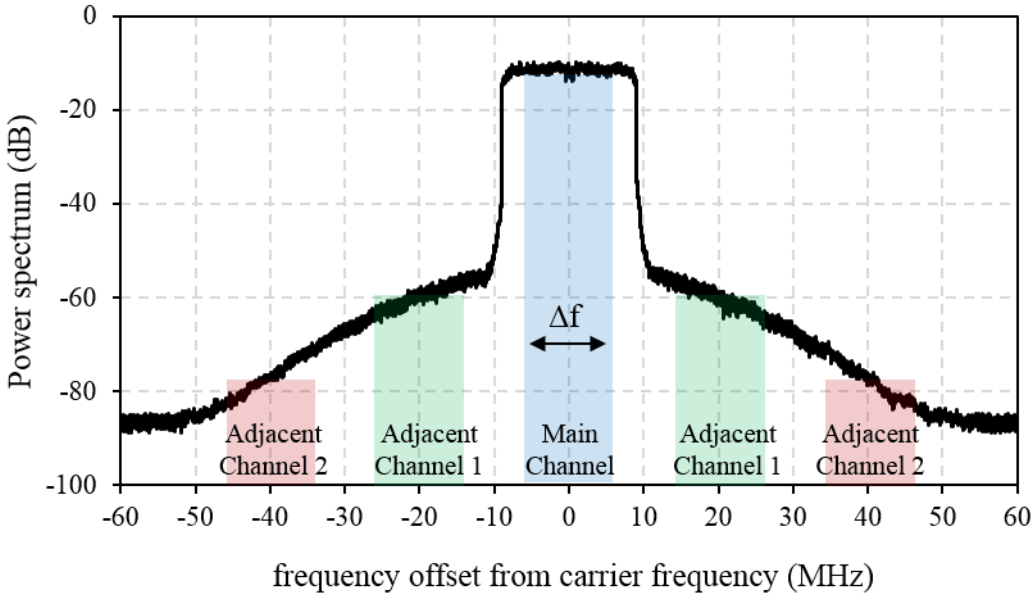



**Figure** 2.6 Definition of adjacent channel power ratio (ACPR)

Adjacent Channel Power Ratio (ACPR) is a ratio of power between the main channel and adjacent channel. It measures the leakage power in adjacent channels, caused by nonlinearities in PAs.

$$ACPR\ 1\ (dBc) = \frac{Power\ in\ Main\ Channel}{Power\ in\ Adjacent\ Channel\ 1} \tag{2.9}$$

$$ACPR\ 2\ (dBc) = \frac{Power\ in\ Main\ Channel}{Power\ in\ Adjacent\ Channel\ 2} \tag{2.10}$$

The poor ACPR means that some energy that is supposed to be in main channels leaked to adjacent channels. It results in reducing the efficiency of signal transmissions.

### 2.5.3 Error Vector Magnitude (EVM)

EVM is another important PA linearity indicator that shows the quality of digitally modulated telecommunication signals. EVM designates the difference between the expected complex voltage value of a demodulated symbol and the value of the actual received symbol. EVM can be calculated using (2.11)

$$EVM\ (\%) = \sqrt{\frac{P_{error}}{P_{reference}}} \times 100 \tag{2.11}$$

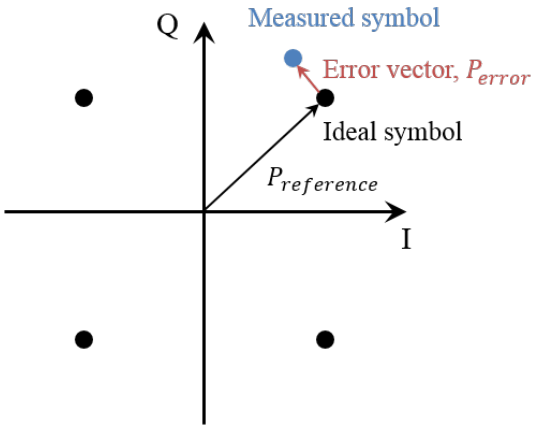



**Figure 2.7** Normalized constellation diagram for QPSK

## 2.6 PA Linearization

### 2.6.1 Linearization Techniques

Modern telecommunication systems, which put a premium on spectral efficiency and a high data rate, call for extremely tight linearity requirements. Due to the latest wireless communication standard, a highly-linear PA is required. However, it is a challenge to operate a PA close to saturation, where amplitude and phase nonlinearities are dominated, to achieve high efficiency for long battery life. A PA linearization allows more efficient use of PAs by compensating the nonlinear distortion produced by PAs. PA linearization techniques can be classified as follow: device [17], circuit [18-19], and system level approaches [20-23]. However, the device and circuit level approaches are not suitable for linearizing PAs with high PAR signals. Therefore, only the system approaches will be introduced since spectrum-efficient 3G/4G modulation schemes show high PAR.

System level approaches are categorized as three groups: feedback, feedforward, and predistortion. A feedback (FB) technique in Figure 2.8 is the simplest method of reducing the distortions of PAs, but the electrical delays around the feedback loop limits the correction bandwidth. Correction bandwidth refers the bandwidth of signals that can be linearized. As the bandwidth of RF waveforms increases, more correction bandwidth is needed in PA linearization. Therefore, PA linearizations using feedback loop show limitations for use in today's wideband RF signals such as LTE, LTE-A, and WCDMA [21].

On the other hands, feedforward (FF) techniquse provide a better IMD correction than FB techniques because FF technique does not suffer from loop delays. Figure 2.9 describes a FF PA.

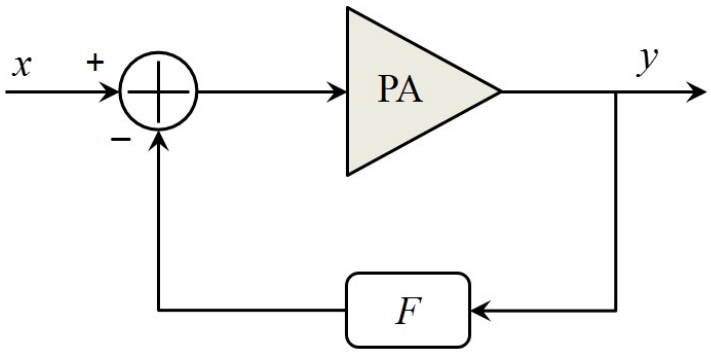



**Figure 2.8** PA linearization with a feedback technique

However, changes of device characteristics with time and temperature are not corrected since it is not closed loop architecture, and the distortion caused by error power amplifier (EPA) may lead another distortion in output signals. Also, the power of EPA must be low enough to keep the overall efficiency [24].

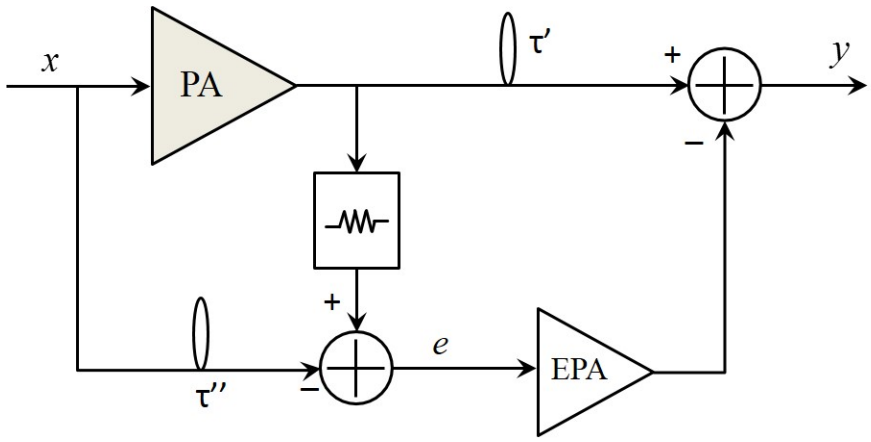
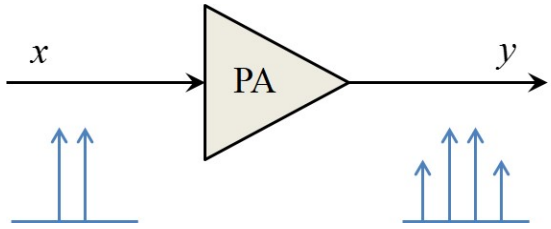


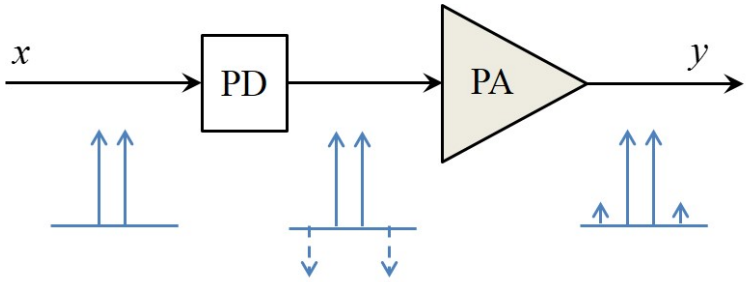

**Figure 2.9** PA linearization with a feedforward technique

Predistortion is the technique that cancels out nonlinearities of PAs by creating a distortion characteristic precisely opposite to that of PAs. As shown in Figure 2.10 (b),

the predistortion (PD) block is placed before a PA. If IMD products generated by predistorter has exactly equal amplitude and out-of-phase to that of a PA, then IMD products caused by a PA can be ideally canceled out.




(a)




(b)

**Figure 2.10** Fundamental operations of PA predistortion (a) PA without linearization technique (b) predistortion techniques at an input of a PA

Table 2.1 summarizes three linearization techniques. Out of the techniques, the predistortion method is a low-cost solution that provides a moderate performance improvement, and it has the additional advantages of low-power consumption and simple circuit configuration over feedforward systems. This technique also provides wider bandwidth in comparison with feedback systems. In past decades, DPD had been a popular method to linearize PA, but it started to show their limits as RF signals employ a

wider BW and more efficient modulation schemes. This research focuses on predistortion among those techniques, especially analog predistortion (APD).

**Table 2.1** Comparison of system-level PA linearization techniques

| Technique | Distortion Cancellation | Bandwidth | Efficiency | Size |
|---|---|---|---|---|
| Feedback | Low | Low | Medium | Medium |
| Feedforward | High | High | Low | Large |
| Predistoriton | Medium | High/Medium | High | Small |

2.6.2 Digital Predistortion

DPD, initially reported in 1983 [25, 26], has been widely investigated and became one of the most fundamental building blocks in modern wireless communication systems. DPD has been more popular and showed superior performance when compared to APD because a DSP is faster, more accurate, and flexible in handling data than analog signal processing.

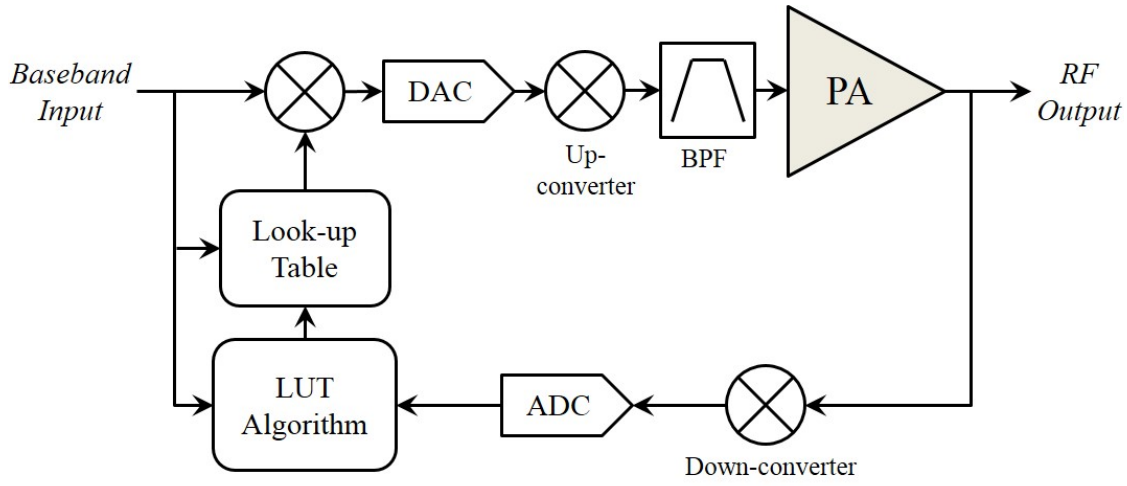



**Figure 2.11** Digital predistortion (DPD)

However, one of the shortcomings of DPD is its extended bandwidth at the beginning of the signal chain: the digital baseband. This has become a significant problem, as a channel bandwidth of RF signal gets wider. Clock speeds need to be five times larger than the bandwidth of RF signal to correct distortion up to fifth order IMD product. With the trend of endlessly increasing the bandwidth of RF signals, high clock speeds burdens the entire DPD system, leading to high power consumption and system complexity. This complexity and power requirements in DPD have precluded its use in small (nano, pico, etc.) base station and mobile phones.

### 2.6.3 Open-loop Analog Predistortion

Despite the outperforming linearization performance of DPD, there have been constant efforts to develop an analog linearization method to solve the problems that DPD has. The IMD components of predistortion circuits should have an exactly equal magnitude and out of phase compared with those of the main amplifier to effectively compensate nonlinearities. However, it is difficult to match the nonlinear characteristic of the predistorter and main amplifier (that needs to be linearized) because they differ in the size and number of stages. Since analog circuits are not as accurate as digital circuits, most analog predistorters have focused on reducing the third-order IMD (IM3) component of PAs. Therefore, a cubic predistorter was used to help reduce third order IMD products generated in a PA. The block diagram of a cubic predistorter is shown in Figure 2.12. The order and placement of many components in a cubic predistorter are not important.

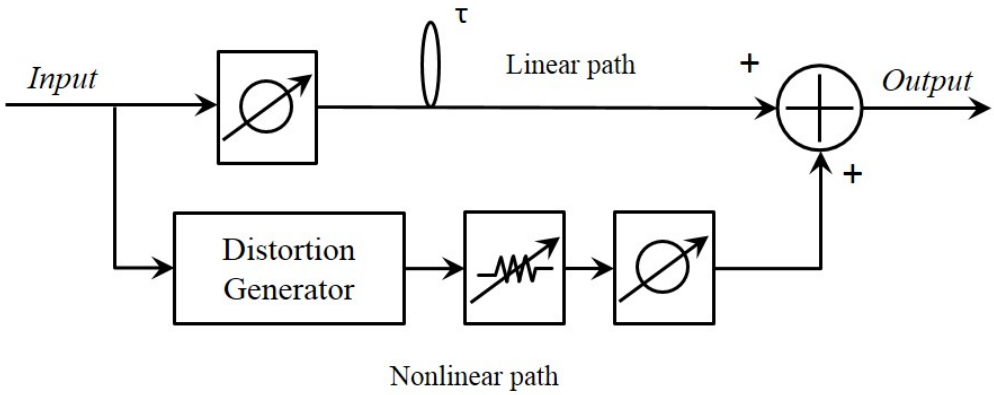



**Figure 2.12** Block diagram of a cubic predistorter

There are two paths in Figure 2.12. The RF input is split between these two paths, nonlinear and linear paths, and recombined before the PA. The nonlinear path consists of a distortion generator, a phase shifter, and an attenuator. The distortion generator typically includes an antiparallel diodes pair that theoretically adds only odd order distortion [27] or an amplifier that tends to saturate at the operating signal levels. The attenuator and phase shifters adjust the third-order IMD products generated by the distortion generator to have an equal amplitude and out-of-phase of that of the PA.

This cubic predistortion was popular for use in linearizing travelling-wave-tube (TWT) amplifiers because these amplifiers usually possess predominantly third-order characteristics. However, since the cubic predistortion may increase the higher-order distortions and the maximum achievable linearity is limited by the higher-order intermodulation products [28], this predistortion is not appropriate for use in high-power solid-state power amplifier application that exhibits considerable high-order IM terms and a memory effect.

A fifth-order predistortion that suppresses both the IM3 and IM5 of a PA has been developed and reported by [29-32]. Fifth-order predistortion linearizers are based on a cubic predistorter but have nonlinear paths more than one. The block diagram of this type linearizer is shown in Figure 2.13.

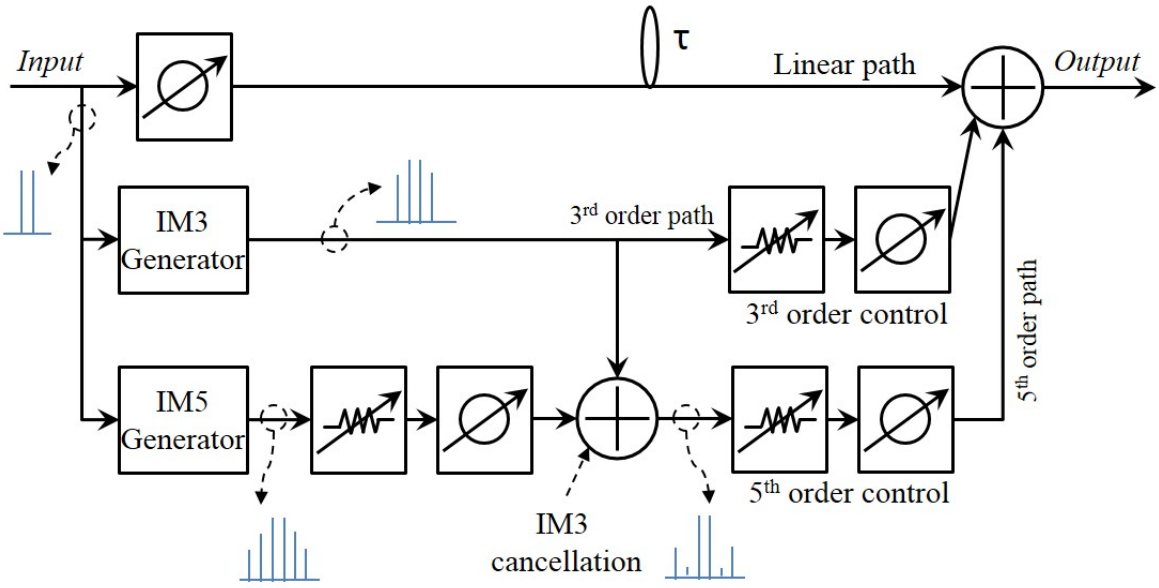



**Figure 2.13** Block diagram of a fifth-order predistorter

However, the fifth-order APDs result in bulky size complex circuitry, a control parameter, control sensitivity, or delay mismatch.

There is another class of analog predistorters that compensates directly for AM-AM and AM-PM nonlinearities of PAs. Typically, amplifiers driven into their nonlinear regions exhibit gain compression (AM-AM) and phase advance (AM-PM) as in red line plots of Figure 2.14. Thus, if the predistorter in Figure 2.14 provides positive amplitude and negative phase deviation with the increase of input power, illustrated in the blue line

plot of Figure, overall PA predistortion systems ideally does not show AM-AM and AM-PM distortions of PAs.

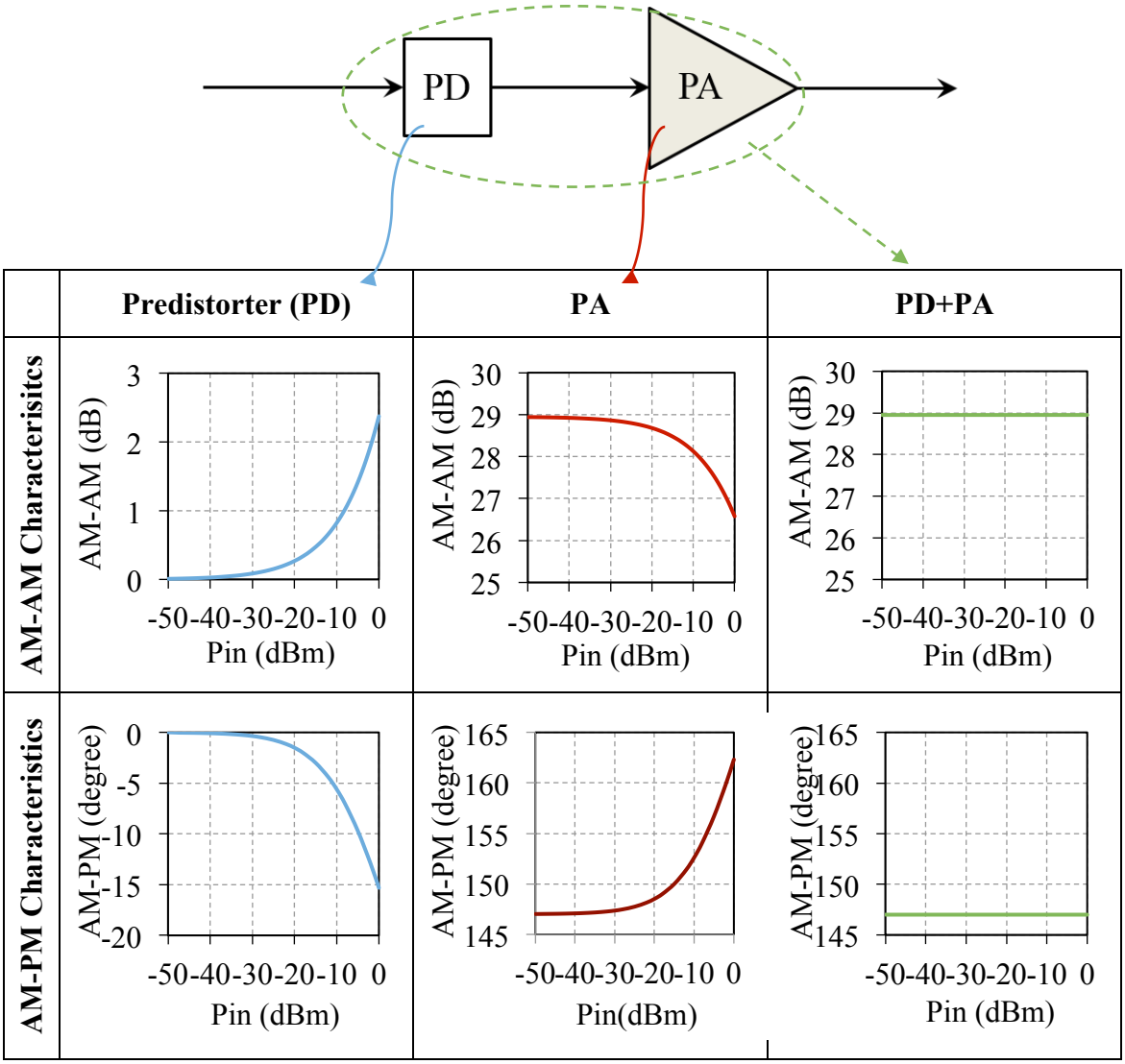



**Figure 2.14** PA predistortion utilizing AM-AM and AM-PM nonlinearities of a PA

A wide variety of circuits that show positive amplitude and negative phase deviation with an increase of input power were proposed and invested. The first example is diode-based predistortion linearizers that utilize the nonlinearity of the resistance of the series diode [33-35]. Likewise, FET-based predistortion linearizers utilize the nonlinearity of transconductance [36-38].

This technique is rather simple, and could be easily integrated with a PA in one package. The difficulty in these predistortion methods is in designing a circuit that will accurately produce a characteristic opposite to the original distortion. Therefore, the linearity improvement reported is very limited and usually suitable for linearizing the nonlinearity of solid-state power amplifiers that have a gain compression and a phase advance characteristics.

Moreover, it cannot be used to linearize a PA with high memory because AM-AM and AM-PM curves of PAs are the memoryless nonlinearities. Moreover, the distortion generators used in the cubic predistorters, the fifth-order predistorter, and a diode or FET-based predistorter generates symmetrical predistorted signals. Also, constant IM3 signals over the modulation frequency ranges are generated to linearize PAs. However, the amplifier's distortion vectors are not constant but vary as a function of modulation frequency. Above APD showed limited linearity improvement since memory effects of PAs are identified as the asymmetry between the lower and upper band in response to the modulation frequency of RF signals [39].

Furthermore, there is no feedback in these open-loop techniques; thus, it is an open-loop system. This means that the distortion to be canceled out must be known in advance, and an open-loop system cannot correct the distortions in PAs that change over time.

2.6.4 Closed-loop Analog Predistortion

Closed-loop predistortion essentially adapts the open-loop predistortion techniques described above to account for variation in the PA's distortion characteristics over time. Conventional predistortion architecture is shown in Figure 2.15. One difference when compared to DPD is that signal predistorting is done in an RF domain, not a baseband domain. Therefore, it does not require DAC or ADC, downconverters, which are needed in DPD.

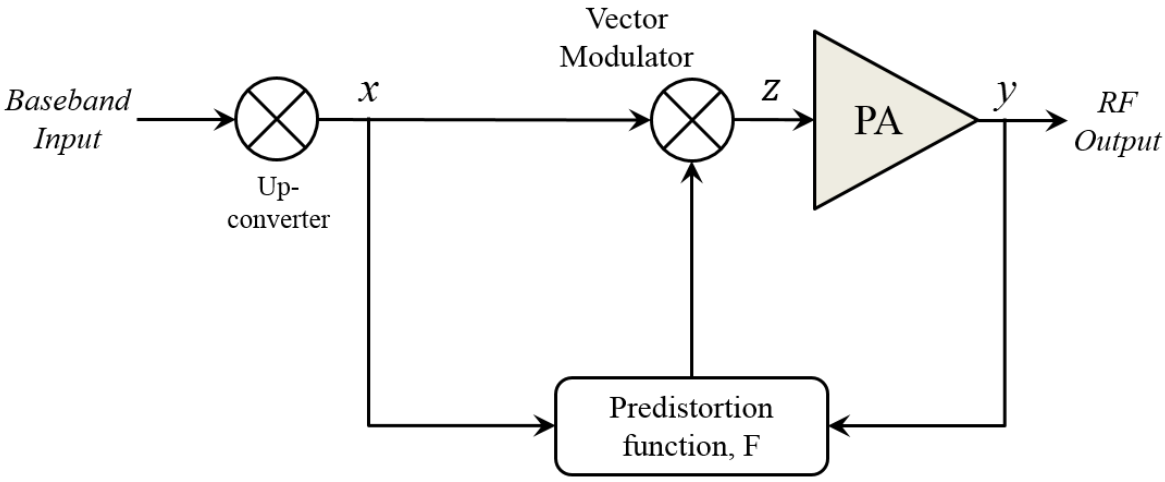



**Figure 2.15** Architecture of a conventional predistortion PA

This architecture compares x and y to calculate the predistortion function, F, and controls the vector modulator shown in Figure 2.15. However, as [21] explored, calculating F is not straightforward. It is difficult to implement this architecture using only analog components. Thus, the DSP algorithm with a look-up table (LUT) is utilized to deliberately implement F. In 2004, Woo et al. proposed a novel closed-loop direct distortion inversion (DDI) that employed commercially available low-power analog

components, as shown in Figure 2.16 [21]. It extracts the nonlinearities of a PA by comparing a magnitude and an phase of signals at the input and output of a PA. The prototype board of this architecture showed an ACPR improvement of 11 dB with a 0.5 W PA when a cdmaOne signal having a PAR of 5.6 dB was applied.

However, the main limitations of linearization performance stem from its correction loop delay, inaccurate analog components, and non-ideal vector modulation characteristics. Furthermore, analog components in this architecture must be much faster and more accurate to cope with today's modern and complex modulation schemes that exhibit a wider BW and a higher PAR.

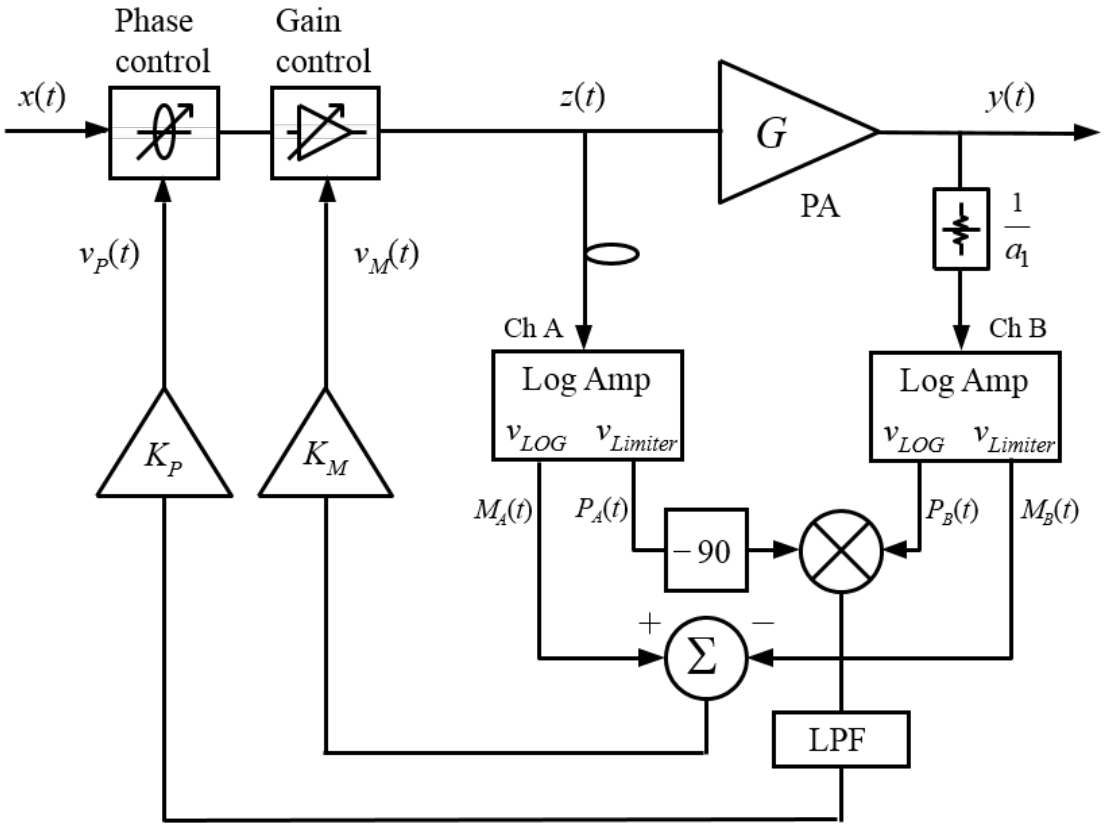



**Figure 2.16** Block diagram of prototype board of APD using the DDI technique [16]

Therefore, a programmable analog signal processing technique that effectively combines digital programmability has been developed to resolve the limitations of all-analog signal processing. Figure 2.17 shows the hybrid architecture that provides a compromise between analog predistortion and baseband DPD [22]. The block diagram of a digitally controlled adaptive analog predistorter is shown in Figure 2.18 [40]. However, supplementary blocks, such as data converters and gain detectors, increase the entire system's power consumption and the system area, thus making it difficult to apply to handset PAs.

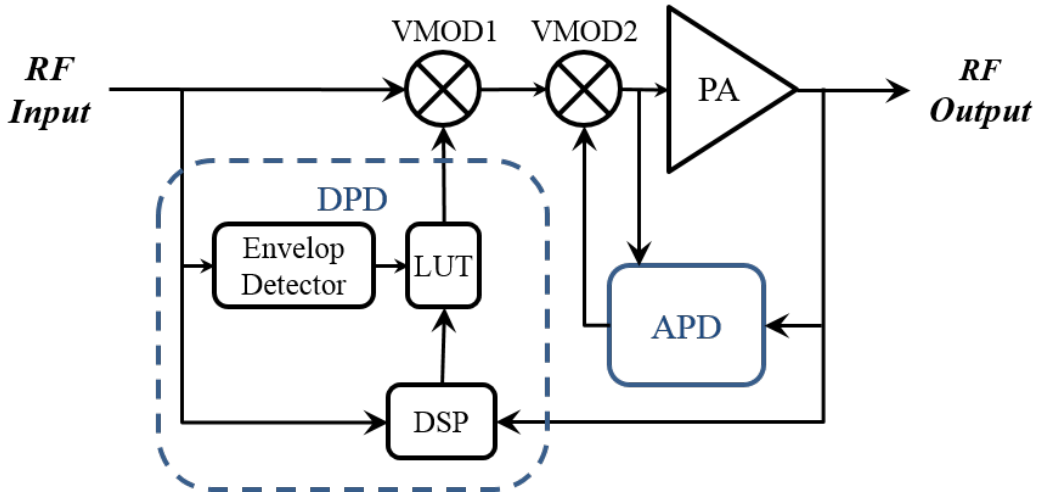



**Figure 2.17** Hybrid DPD/APD predistortion PA [22]

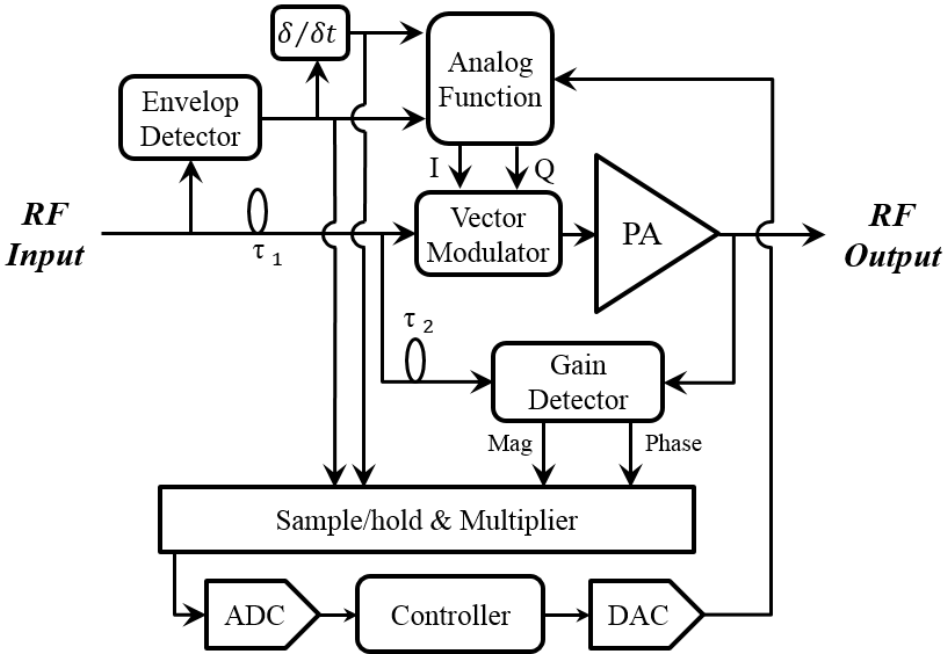



**Figure 2.18** Digitally-assisted APD [40]

# CHAPTER 3

# PA PREDISTORTERS

## 3.1 Introduction

The purpose of this research is to investigate ways to implement the predistortion of PA in the form of analog circuits or systems. In particular, this research has focused on designs that provide higher levels of performance required by 4G cellular systems. In this chapter, analog control circuits, variable phase shifter (VPS) and variable gain amplifier (VGA) customized for APD, are investigated and explored.

## 3.2 Requirements for Analog Predistorters for Use in Analog Predistortion of RF PAs

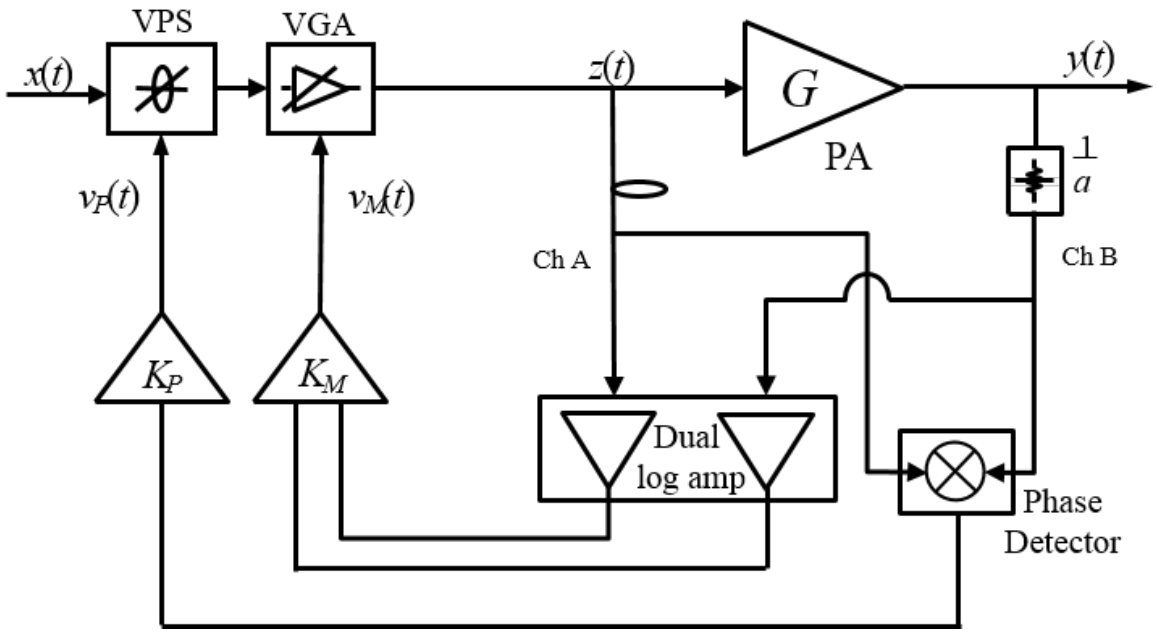



**Figure 3.1** Revised analog predistortion PA system

Based on the APD architecture in [21], the revised APD architecture is illustrated in Figure 3.1. A VVA, variable-voltage amplifier, is replaced with a variable gain amplifier (VGA), and dual log amplifier is the single die that has two same log amps since two log amps on the same die matches better than the two log amps on two individual dies respectively. A phase detector is placed in this system to detect AM-PM errors in a PA. Computer simulations were conducted to determine the required specifications of each component specifically for use in LTE cellular systems.

This APD architecture has five major components: VPS as a phase controller, a VGA as an amplitude controller, logarithmic amplifiers (log amps) as power detectors, a phase detector (PD), and a loop control circuitry. To achieve adequate linearization in this APD, there are special demands on these components, which are not typical concerns for other applications that may use similar components. In this section, required specifications of the PA predistorters such as VPS and VGA will be explored.

First of all, components in the RF chain from x(t) to y(t) need to cover entire LTE frequency bands to develop an APD systems for use in LTE cellular systems. Required operating frequency range of cascaded VPS and VGA has to be, at least, from 700 MHz to 2.4 GHz to cover most of the present and proposed cellular bands.

Secondly, since the AM-PM errors in most PAs are smaller than 20° [41-44], the VPS in the APD application does not need a wide range of phase control, but does need very accurate phase control to maximize AM-PM error compensation. Similarly, because the AM-AM errors of most PAs are limited to a few dB over excursion of the envelope, the gain control range of VGA needs to only cover the range of the input amplitude for

which significant gain compression (saturation) occurs. Through exhaustive simulations, it has been determined that the VGA needs a gain control range of 5 dB ~ -10 dB.

While the required amount of phase control of VPS and that of amplitude control range of VGA are relaxed when compared to other application, these components in APD have to be very accurate to achieve adequate linearization. Moreover, the gain variation of VPS has to be as low as possible not to introduce amplitude errors from VPS and not to exacerbate the AM-AM errors in PAs. It has been decided that the gain variations of the VPS should be less than a 0.1 dB per 1° phase shift through simulations. Similarly, the phase shifts of VGA must be less than 5° over the gain control from 5 dB to -10 dB.

Lastly, the requirement on modulation BW of VPS and VGA must be at least 100 MHz and 60 MHz respectively to accommodate a modern wireless waveform. Note that AM-PM errors in PAs extend mostly within five times of the I/Q BW. Likewise, AM-AM errors extend mostly with three times of the I/Q BW.

Based on the determined specification in Table 3.1, customized VPS, VGA and log amp for the APD application has been developed. The design process and its simulation, measurement results will be described as below.

**Table 3.1** Requirements of analog parts in analog predistortion

| | **VPS** | **VGA** |
|---|---|---|
| **RF Freq.** | 0.7 GHz – 2.7 GHz | |
| **Bandwidth** | Modulation BW<br>> 100 MHz | Modulation BW<br>> 60 MHz |
| **Accuracy** | 20° phase control with error ≤ ±1° | 5 ~ -10 dB gain control with error<br>≤ ± 0.5 dB |
| **Other** | Gain variation ≤ 0.1 dB/1° | Phase variation ≤ 5° |

## 3.3 Phase and Amplitude Control Circuits

As mentioned before, there are special demands on a VGA and a VPS as an amplitude and a phase predistorter in APD, which are not concerns in typical designs. This section will focus on designing the fast and accurate analog VPS and VGA.

### 3.3.1 Variable Phase Shifter

A VPS design having a modified poly-phase filter (PPF) was proposed in [45]. However, it approached the VPS design only from a linear controllability and didn't fully go through the all of the requirement that a VPS needs for an APD linearization system. The work presented in this section focuses on other aspect of VPS, such as its modulation BW [46]. Figure 3.2 illustrates the schematic of VPS that consists of a PPF, a phase controller, and a vector-sum amplifier.

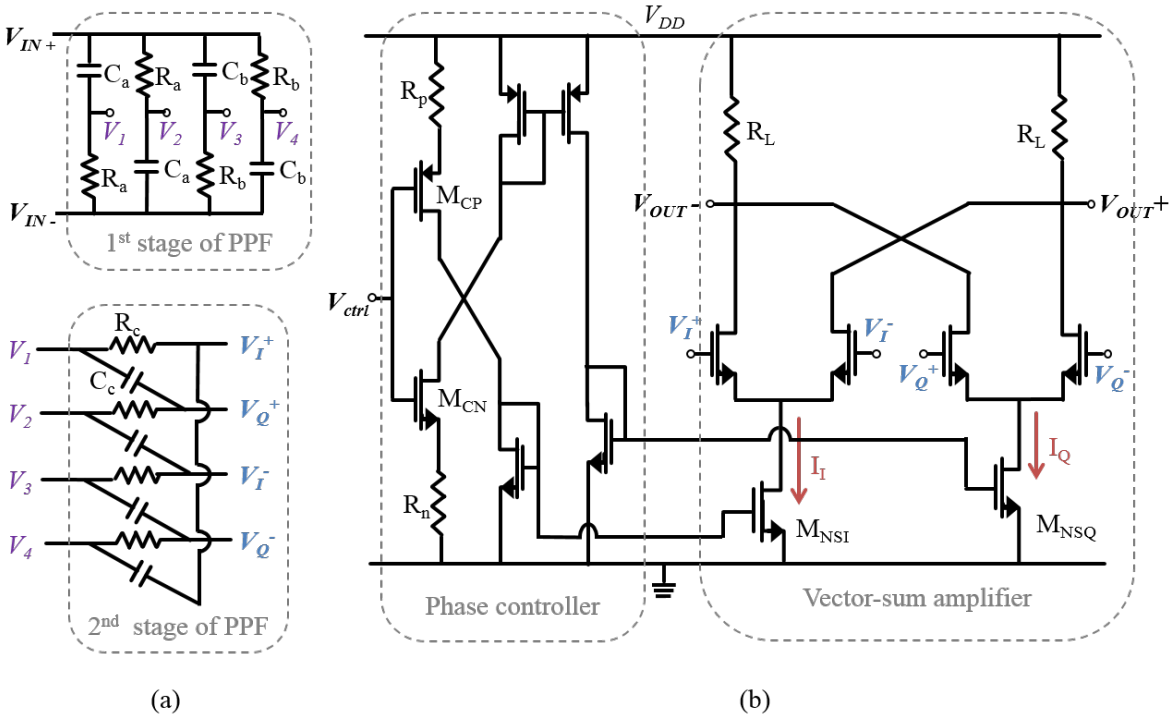



**Figure 3.2** VPS schematics (a) Poly-phase filter (PPF) (b) Phase control circuit and vector-sum amplifier

In Figure 3.2 (a), the phase control signal, $V_{ctrl}$, goes through the control circuit and tail transistors, $M_{NSI}$ and $M_{NSQ}$, of the vector-sum amplifier, so that the input $V_{ctrl}$ modulates the RF signal from a single control voltage. When $V_{ctrl}$ is at the low end of the control voltage range, the current $I_Q$ shown in Figure 3.2 becomes less than current $I_I$. Under this condition, the quadrature (Q) branch in vector-sum amplifier starts limiting the modulation BW. On the other hands, the in-phase (I) branch starts limiting the modulation BW as $V_{ctrl}$ is at the high end of the control voltage range. VPS design in [45] showed much lower modulation BW than our target specification in Table 1 because the sizes of $M_{PC}$, $M_{NC}$ in the phase controller were large, and the gate capacitances of these transistors limited the speed of the phase controller. Therefore, the size of $M_{PC}$, $M_{NC}$ was decreased enough to speed up the phase controller operation and increase the modulation BW of VPS.

A one-tone signal was applied to the control port while RF signal was applied to RF input port to simulate the modulation BW, as illustrated in Figure 3.3. Modulation BW was determined to the frequency of the control port when the power of sidebands at the output signals of VPS dropped by 3 dB. Figure 3.3 shows the simulation setup of the modulation BW measurements.

It was measured at several different DC control voltage, and it is shown in Figure 3.4 (a). This result shows that the modulation BW of VPS starts to be limited by Q branches in Figure 3.2 (b) when DC voltage of control port is smaller than 0.9 V. Likewise, the modulation BW of VPS is limited by I branch in Figure 3.2 (b) when DC voltage of control port gets larger than 0.9 V.

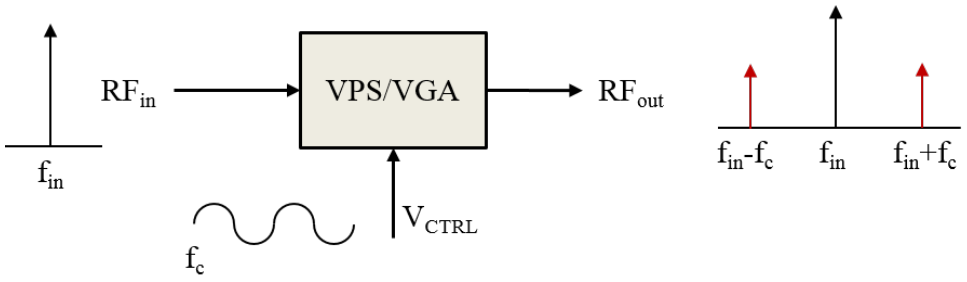
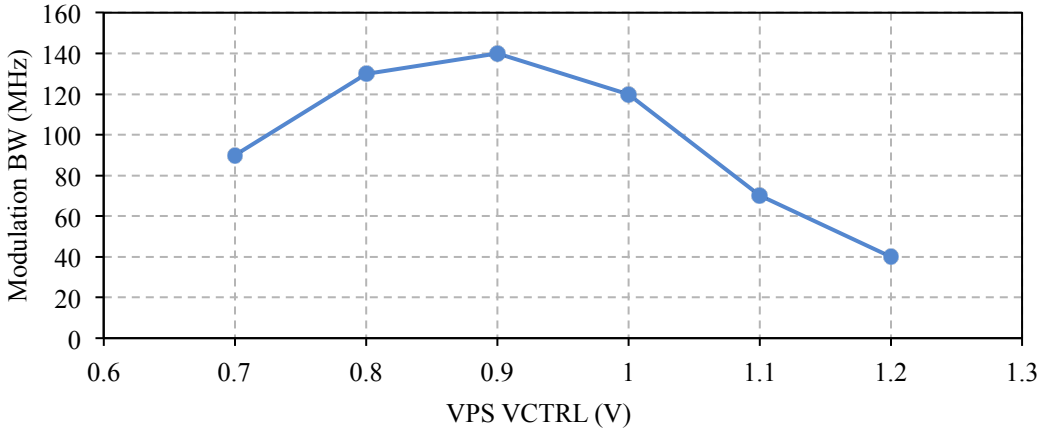
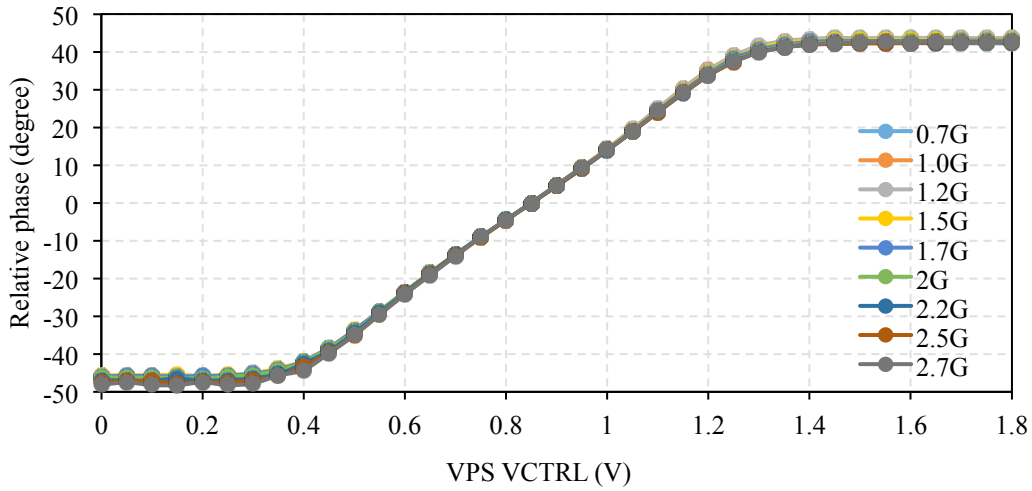



**Figure 3.3** Simulation setting to measure a modulation bandwidth




(a)




(b)

**Figure 3.4** VPS simulation results (a) Modulation bandwidth (b) Phase shifting with VPS Vctrl

Because the VPS for use in APD applications needs only 30° phase control which corresponds to a 0.3 V DC control range of VPS, as shown in Figure 3.4 (b), the effective operating range of VPS control port is from 0.75 V to 1.05 V. At this range, the modulation BW of VPS is larger than 100 MHz, enabling AM-PM correction BW larger than 100 MHz in APD applications.

### 3.3.2 Variable Gain Amplifier

Huang *et al*. proposed the variable gain amplifier that had a continuous, linear-in-dB gain control curve for use in applications such as APD [47]. However, he neglected to consider the modulation BW requirement necessary to implement the APD. Also, he used to triple-well CMOS technology to improve the linearity of his VGA, but a triple-well technology is not available for this study. Thus, in this study, the originally proposed VGA has been improved to provide an adequate modulation BW and an adequate linearity even with twin-well CMOS devices. Figure 3.5 shows the block diagram of the overall modified VGA for APD applications.

First of all, the bottleneck of narrow modulation BW in the VGA came from the narrow BW of the operational amplifier (op-amp) in the attenuator controller in Figure 3.5. In this work, this op-amp was redesigned to have a wider BW so that the overall modulation BW of VGA is improved to meet the requirements shown in Table 3.1.

The VGA work in [47] used the triple-well technology to improve the linearity of VGA, but this technology was not available for this study. Therefore, multi-stacked transistors are used in a shunt branch and a series branch. However, multi-stacked transistors introduce larger capacitance around them, leading to limiting an RF path bandwidth and a large chip size.

Therefore, numbers of stacking devices are adjusted to meet both target RF bandwidth from 700 MHz to 2.4 GHz and required IIP3. It has been determined that two stacked devices for series transistors, and four stacked devices for shunt transistors.

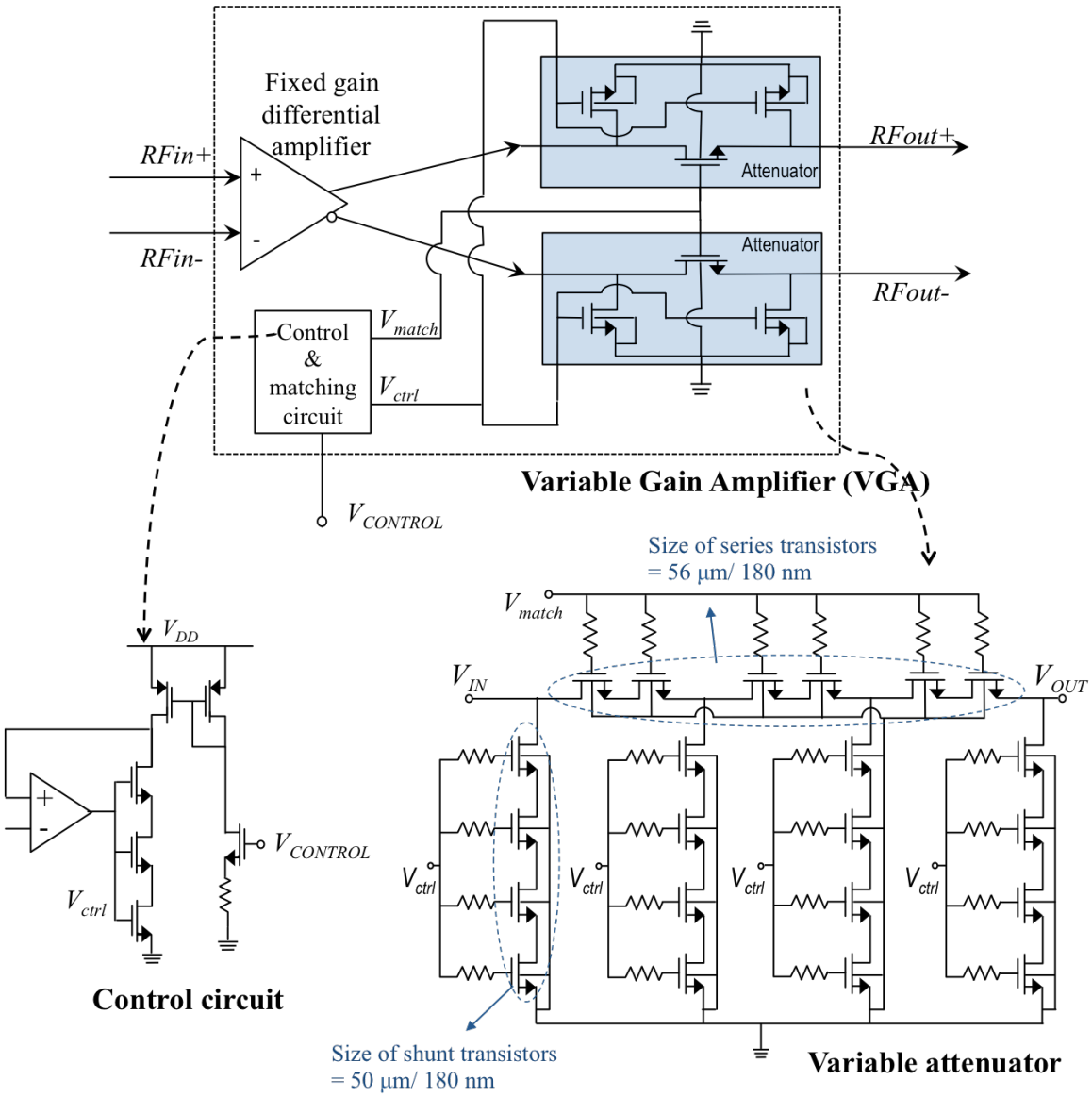



**Figure 3.5** The overall schematic of the VGA design

### 3.3.3 Measured Results of the Cascaded VPS and VGA

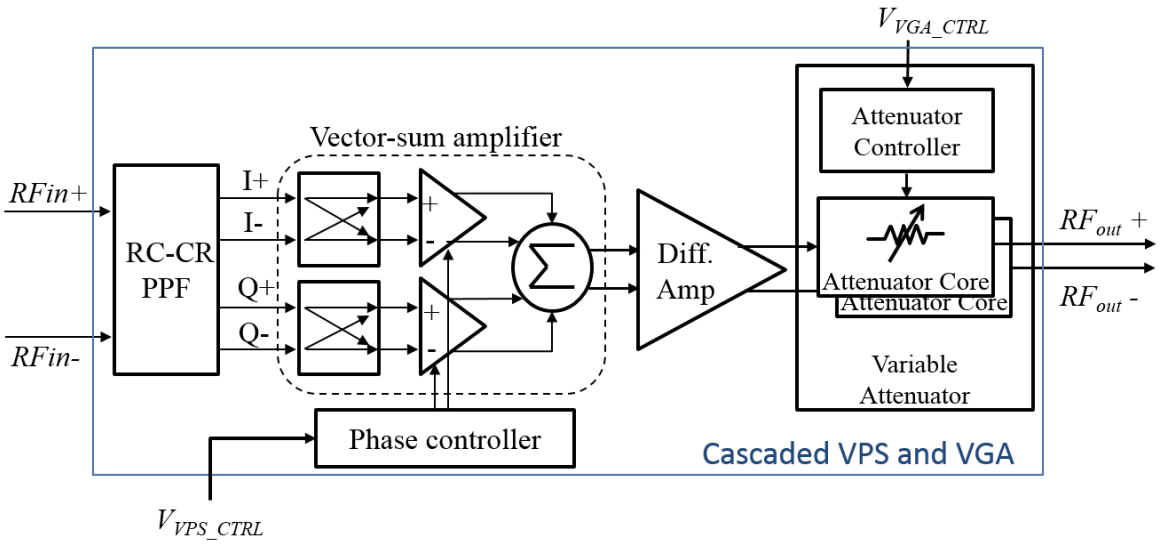
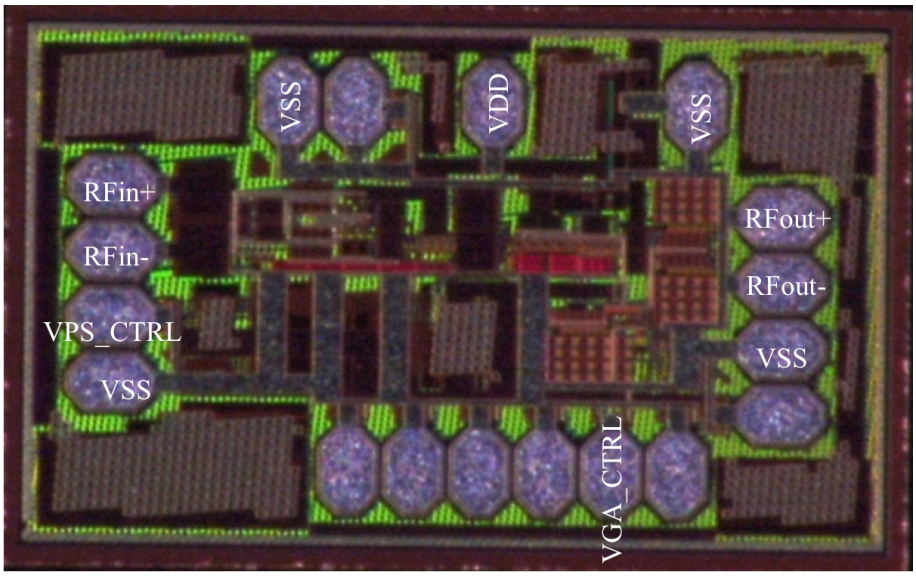
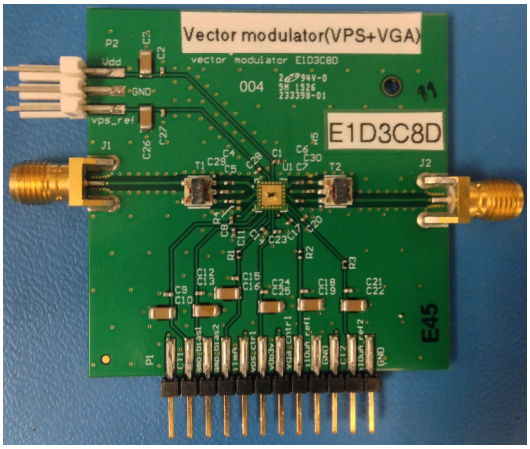



**Figure 3.6** The block diagram of cascaded VPS and VGA

VPS and VGA are cascaded and integrated into one die to reduce the power dissipation at output buffers that drive 50 Ω output loading. Since the variable attenuator in the VGA is already 50 ohm terminated, VPS followed by VGA was designed as shown in Figure 3.6. This combo of VPS and VGA was fabricated using Jazz SiGe BiCMOS 0.18 um process and tested. The fabricated die photo is shown in Figure 3.7 (a) and Test board with the fabricated die of VPS and VGA is shown in Figure 3.7 (b). A transformer (Mini-Circuits TCP-1-43+) is placed at the input port to change single-ended signals to differential signals. Likewise, a transformer at output port change the differential signals coming from VGA to single-ended output signals.



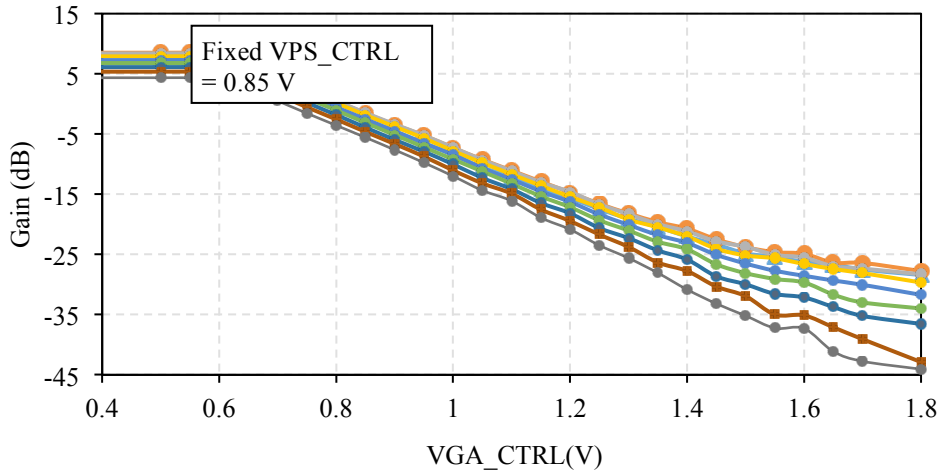

(a)



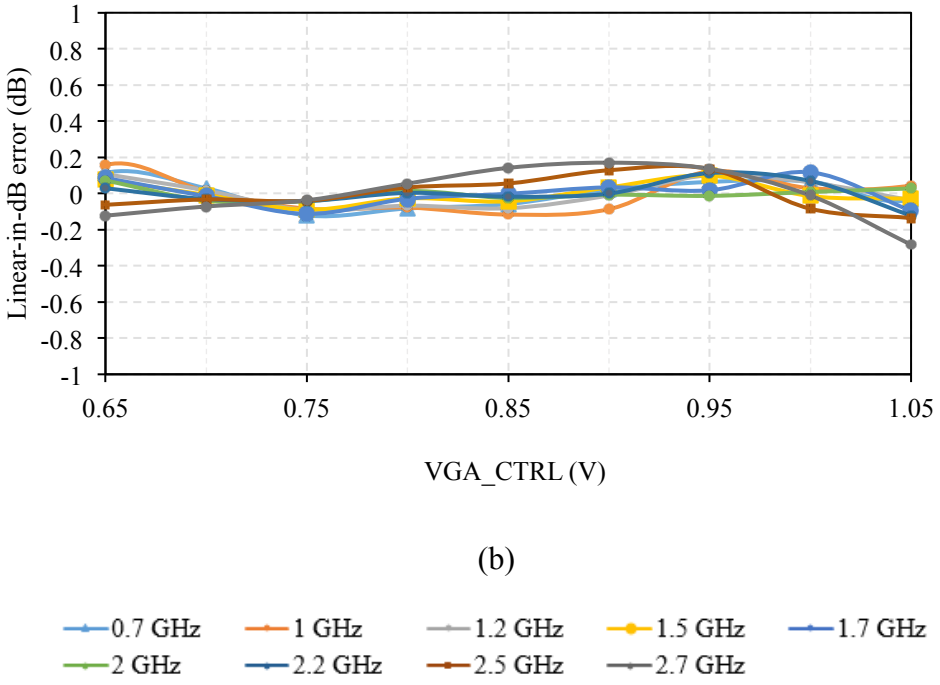

(b)

**Figure 3.7** The fabricated VPS and VGA (a) Die photograph and (b) The test board.

The gain of VGA and phase shifting of VPS with control pins, $V_{VPS\_CTRL}$ and $V_{VGA\_CTRL}$ were measured by network analyzer (Agilent 5071C), and then the loss or phase shifts in the transformers were excluded from the measured data. These data are plotted in Figure 3.8 and Figure 3.9.




(a)

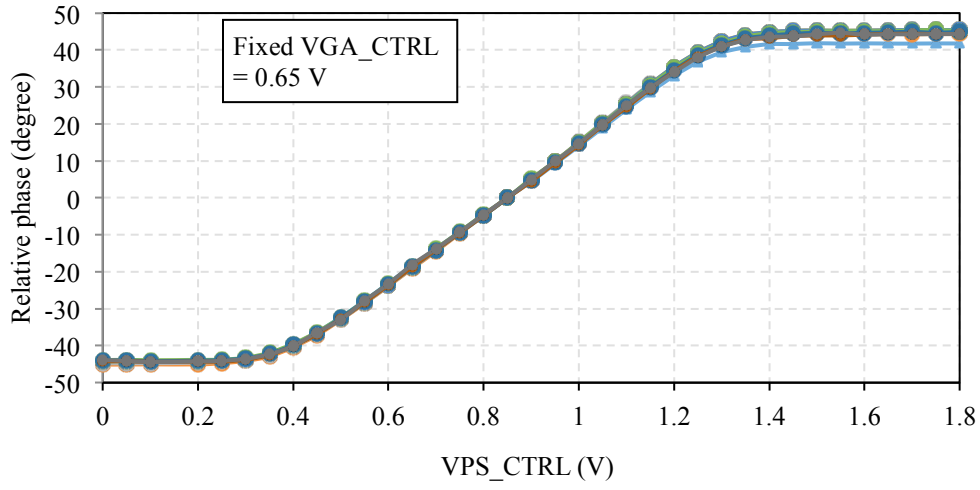



(b)

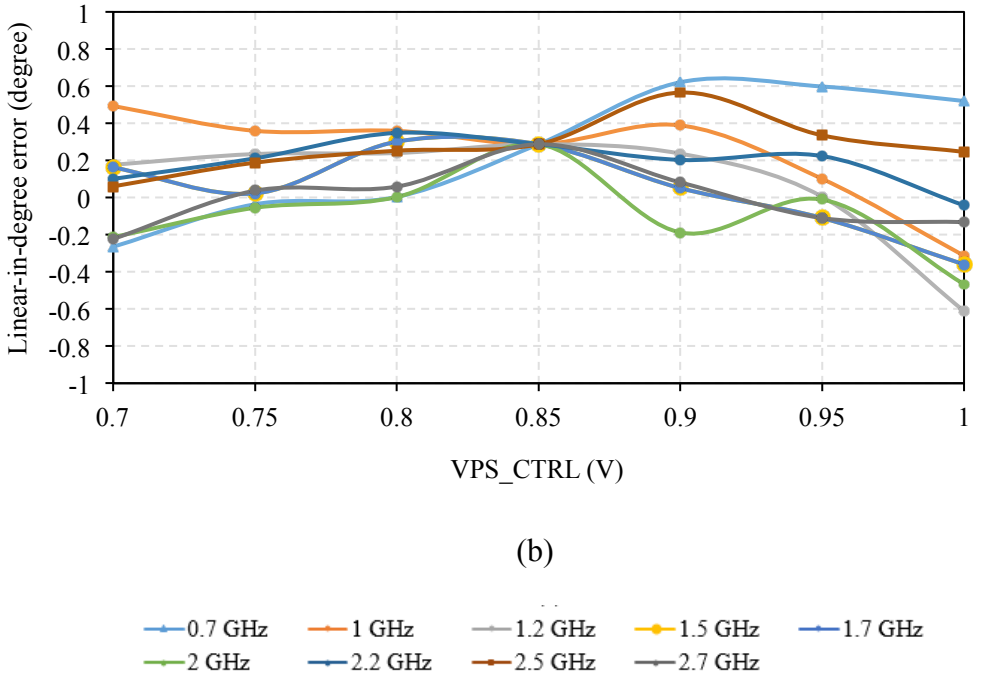
**Figure 3.8** Measured results (a) Total gain vs. VGA_VCTRL (b) Linear-in-dB errors

Even though the gain drops as an RF frequency increases, gain control slopes at different frequencies in Figure 3.8 (a) are similar each other. Each of lines in Figure 3.8 (a) is fitted with straight lines and differences between the lines in Figure 3.8 (a) the straight lines are calculated, linear-in-dB errors, are plotted in Figure 3.8 (b). Computed linear-in-dB error

is less than ±0.3 dB at gain control range from 5 dB to -10 dB. Phase variations with VGA gain control from 5 dB to -10 dB were measured, which is less than 3 degree at an RF 0.7 GHz.




(a)




(b)

**Figure 3.9** Measured results (a) Phase shift vs. VPS_VCTRL (b) Linear-in-degree error

Likewise, the phase shiftings of VPS are measured and plotted in Figure 3.9 (a). These phase control curves at different frequencies in operating frequency from 0.7 GHz to 2.7 GHz are quite similar each other. Linear-in-degree error is calculated by calculating the difference between the lines in Figure (a) and fitted straight lines. Linear-in-degree error is less than ± 0.6° at all operating frequency. Gain variations with VPS phase control of 30° were measured as well and worst case was 0.35 dB at an RF frequency of 1.7 GHz

A one-tone signal was applied to the control ports of VPS and VGA while 1 GHz RF signal was applied to the input port to measure the modulation BW. Modulation BW was determined to the frequency of the control port when the power of sidebands at the output signals of VPS and VGA combo dropped by 3 dB. Measurement results are plotted in Figure 11. Figure shows the experimental setup of the modulation BW measurements. The modulation BW of the VPS is larger than 90 MHz, which is less than the target in table 1 but still acceptable for use in APD application. The modulation BW of the VGA was larger than 70 MHz, which meets the target.

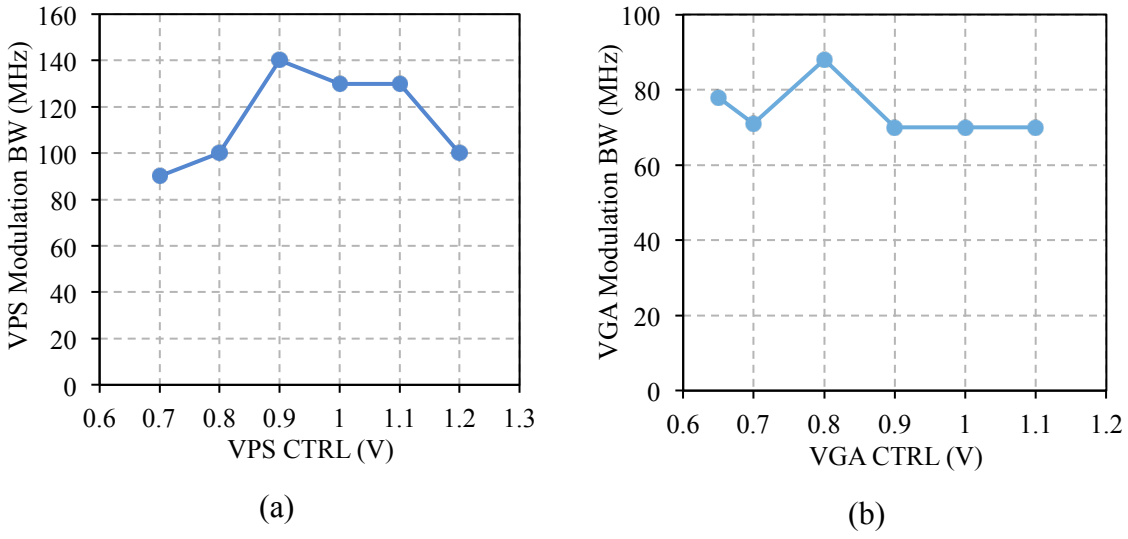



**Figure 3.9** Measured modulation BW (a) VPS (b) VGA

Table 3.2 summarizes the overall measured results and compares them with the targets that previously determined at Table 1. The symbol of represents that a measured result meets the target specification, and the symbol represents that measured results do not exactly meet the target but still acceptable for use in APD systems.

**Table 3.2** Measured performance summary of VPS and VGA

| **Quantity** | **Target** | **Measured data** |
|---|---|---|
| DC current | | 31.82 mA |
| Power | | 57.28 mW |
| Frequency | 700 M-2.4 GHz | 510 M – 2.4 GHz |
| Total phase control range | | 88.6◦ (typical)<br>86.5◦ (0.7 GHz) |
| Linear-in-degree error at 30◦ phase control range | < ± 1◦ | ±0.62◦ |
| Gain variation at 30◦ phase control range | < 3 dB | max 0.35 dB at 1.7 GHz |
| VPS modulation BW at 30◦ phase control range | 100 MHz | 90 MHz |
| Total gain control range | | 5~-30 dB |
| Linear-in-dB error at 5 ~ -10 dB gain control range | < ±0.5 dB | ±0.25 dB |
| Phase variation at 5 ~ -10 dB gain control range | max 5◦ at 2.7 GHz | max 9◦ at RF 2.7 GHz |
| VGA Modulation BW | 60 MHz | 70 MHz |
| Input referred IP3 | | -7.49 dBm at RF 1.2 GHz |
| Input referred P1dB | | -18.44 dBm at 1 GHz |

According to the table, this VPS/VGA is designed enough for use as a phase and amplitude predistorter in the APD.

# CHAPTER 4

# PA ERROR DETECTORS

## 4.1 Introduction

As shown in Figure 3.1, the APD system utilizes logarithmic amplifiers (log amps) to detect the AM-AM error of the PA. Likewise, this system uses a phase detector to detect the AM-PM error of the PA. To maximize the cancellation of this error, there are special demands on these log amps and the phase detector. In this chapter 4, above all, the required specifications of the PA error detectors for use in APD applications will be presented. Then, the focus will be on log amp design because Qorvo, Inc. helped design the phase detector for use in APD applications and this phase detector will be used later when implementing APD systems. The design process of the log amp is presented, and its measured data from the fabricated circuit is shown as well.

## 4.2 Requirements of PA Error Detectors for Use in Analog Predistortion PA System

In this section, the required specifications of PA error detectors such as log amps [48] and phase detectors will be presented and the design of the log amp has been done based on these specification at the later sections.

First of all, the video bandwidth (VBW) of log amp in APD must be as high as 60 MHz since the signal amplitude is detected. Also, the response delay of the log amp plays a significant role in determining the overall correction BW [21]. We have determined that

its response time must be less than 3 ns to achieve a 60 MHz correction BW through excessive system simulations. Add accuracy with simulation results.

Lastly, the important properties of the phase detector (PD) in the APD are the accuracy of its output and the amount of its group delay. The required specifications have been determined through the simulation. Above information is summarized in Table 4.1. It includes the target specifications of the critical analog parts in APD system used for correcting a 20 MHz BW LTE signal over operating frequency range of 0.7 GHz – 2.7 GHz, covering all proposed and present cellular frequency bands.

Since the AM-AM errors of most PAs are usually limited to a few dB over the excursion of the envelope, the dynamic range requirements need to only cover the compression over the range of peak-to-average power ratio (PAR) of the input waveform. It has been determined that 20 dB input dynamic range is sufficient for the APD application. But while the dynamic range is relaxed when compared to other log amp applications, the detected output must be very accurate to achieve adequate linearization.

**Table 4.1** Determined specifications of PA error detector in APD

| | **Log Amp** | **Phase Detector** |
|---|---|---|
| **RF Freq.** | 0.7 GHz – 2.7 GHz | |
| **Bandwidth** | Video BW > 60 MHz | Instantaneous BW > 100MHz |
| **Accuracy** | 20 dB dynamic range with error < ± 0.5 dB | ± 0.5 % deviation from linear response |
| **Other** | Response time < 3 ns | Group delay < 2 ns |

## 4.3 Circuit Designs of the Logarithmic Amplifier

### 4.3.1 Architecture of the Logarithmic Amplifier

Figure 4.1 shows the block diagram of the proposed log amp designed for APD application. Its architecture is the well-known successive detection log amp.

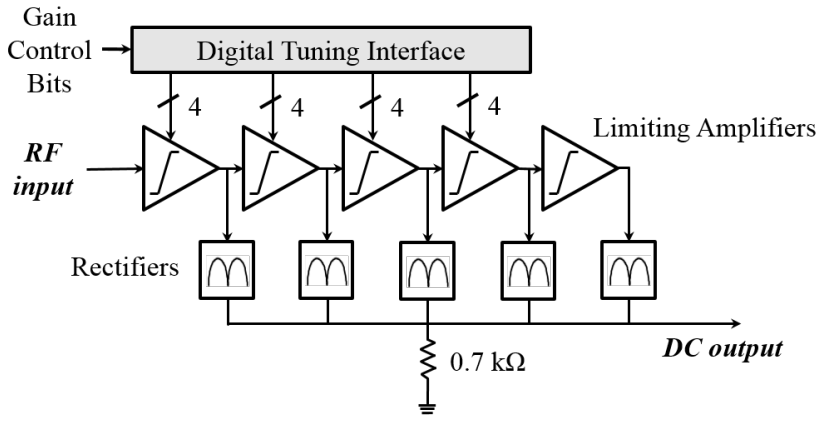



**Figure 4.1** Block diagram of logarithmic amplifier

In order for the APD to cancel out not only IMD products in the RF PA but also any nonlinearity in amplitude control loop of APD, this log amp was designed to be digitally calibrate-able. This is done by controlling the gain of each limiting amplifier to linearize the output characteristic curve of the log amp.

### 4.3.2 Limiting Amplifiers (limiters)

Limiter schematic is illustrated in Figure 4.2 (a). It is the Cherry-Hooper amplifier with emitter-follower feedback, which enables low-power operation with wide RF BW, and has sufficient gain [49]. For the log amp to achieve the required input dynamic range for 20 dB, five stages of limiting amplifiers are used to achieve a total gain of 35 dB and

overall RF BW of 660 MHz – 3.3 GHz. An extra limiter stage is added to provide equal output loading on all stages. In addition, capacitors canceling DC offsets are placed between the limiting amplifiers. The gain of each limiter is controllable by adjusting the tail current of the limiter.

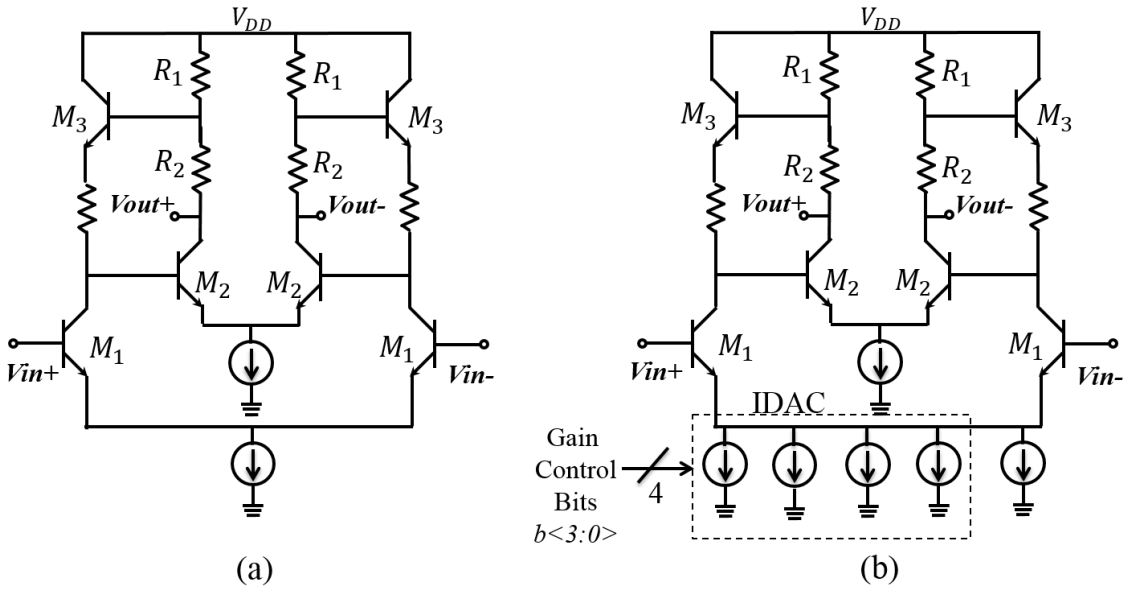



**Figure 4.2** Limiter schematic (a) Without digital calibration capabilities (b) With digital calibration capabilities

For the APD to cancel out not only the intermodulation (IMD) products in RF PA but also any nonlinearity in amplitude control loop of the APD, the log amp is designed to be digitally calibrate-able. To calibrate the shape of the characteristic curve (input RF power vs. output voltage), current DACs (IDACs) are added to adjust each limiter gain by calibrating the current of $M_1$ in Fig. 4.2 (b). According to [49], a gain of this limiting amplifier is proportional to the transconductance of $M_1$, $g_{m,\,M1}$, while BW of the log amp

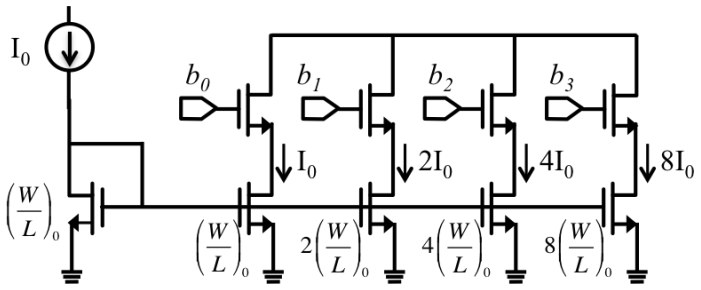



**Figure 4.3** The detailed schematic of IDAC in the limiter design

is independent to $g_{m,\,M1}$ when $g_{m,\,M2}$ x $R_1$ >> 1. As shown in Figure 4.2 (b), the digital tuning interface is implemented to control each IDAC. More detail schematic of IDAC is illustrated in Fig. 4.3. The total controllable gain of each limiter is 1.5 dB and IDAC can make a deliberate gain control in sixteen states. Transfer characteristic of the log amp (Vout vs. Input power) can be deliberately controllable by calibrating each gain of the limiter stages.

### 4.3.3 Full-Wave Rectifiers

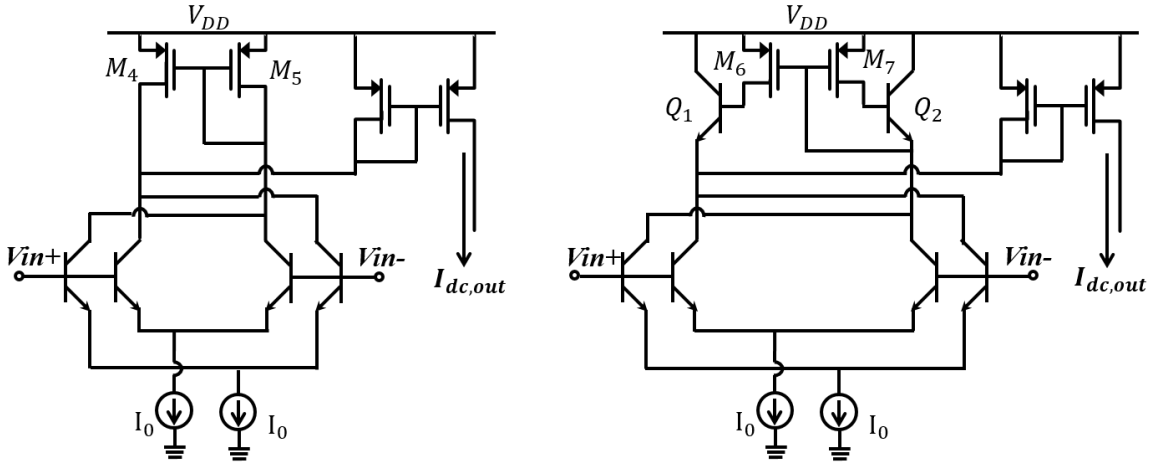



**Figure 4.4** The schematic of full-wave rectifier (a) Conventional rectifier (b) Revised rectifier

Figure 4.4 (a) shows the schematic of a conventional full-wave rectifier using the unbalanced emitter-coupled pairs [50], as presented in [51] and [52]. The bottleneck in log amp VBW and response time is often the relatively slow response of such rectifiers. To make a faster rectifier, we revised it as shown in Fig. 4.4 (b). Compound PMOS/NPN transistors, $Q_1$, $Q_2$, $M_6$ and $M_7$ replaced $M_4$ and $M_5$ in the current mirror in Fig. 4.4 (a).

The idea of combining PMOS and NPN [53] has an effect of scaling up the width-to-length ratio of PMOS by (1+β), without significantly increasing parasitic capacitance. For the conventional circuit shown in Fig. 4.4 (a), when the width of PMOS is scaled up by a factor of (1+β), its parasitic capacitor is increased by a factor of (1+β) as well. This increased capacitance slows down the entire circuit by a considerable degree. The compound PMOS/NPN transistors significantly speed up the rectifier operation, improving the overall response time and VBW of the log amp.

**Table 4.2** Performance comparison between the conventional rectifier and the revised rectifier with a PMOS and NPN composite transistor

| | **Conventional Rectifier** | **Revised Rectifier** |
|---|---|---|
| **Rise Time** | 3.85 ns | 2.08 ns |
| **Video Bandwidth** | 150 MHz | 180 MHz |

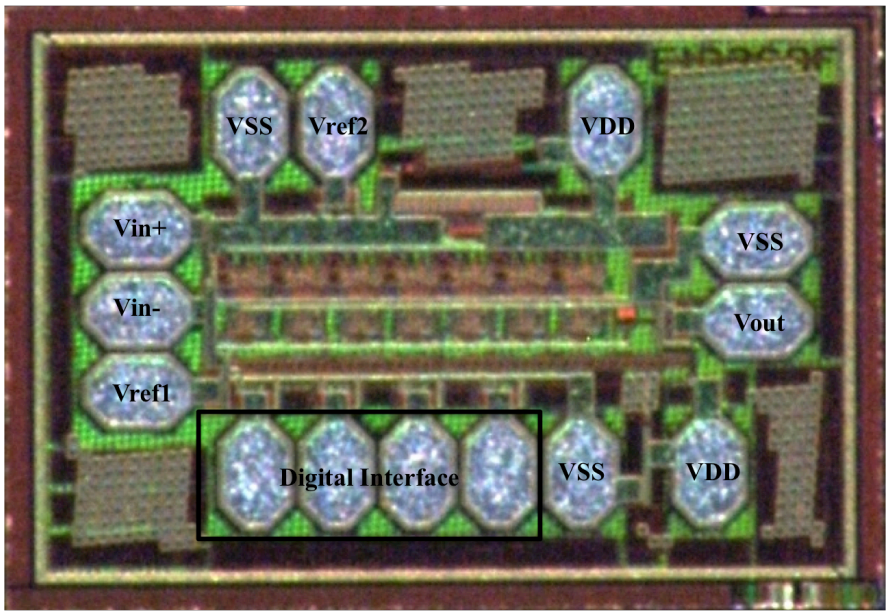
Table 4.2 shows the simulated log amp performance comparison between when using conventional rectifier design as Figure 4.4 (a) and our revised rectifier design as Figure 4.4 (b). When simulating the response time, a constant frequency of RF input was stepped between -50 dBm (the lowest power within the input dynamic range) and -30 dBm (the highest power within input dynamic range). The rise time (10% - 90%) of the

output voltage was then measured. When simulating VBW, an amplitude modulated signal having -40 dBm carrier power and a modulation index of 0.1 was applied and the frequency of the modulating signal was swept. The simulation was done with an output capacitance loading of 1 pF, representing the estimated parasitic capacitance from IC packaging and electrostatic discharge (ESD) protection.

These simulation results prove that the compound PMOS/NPN transistors in rectifier significantly improve the VBW and response time of the log amp.

### 4.3.4 Measurement Results

Designed log amp was fabricated in the Jazz 0.18 um SiGe BiCMOS process and measured. The die photograph of the fabricated log amp and its test board are shown in Figure 4.5 (a) and (b), respectively. This die was packaged in QFN and mounted on PCB for a measurement purpose. A transformer that changes a single-ended RF signal to a differential signal was mounted at the input of the log amp.

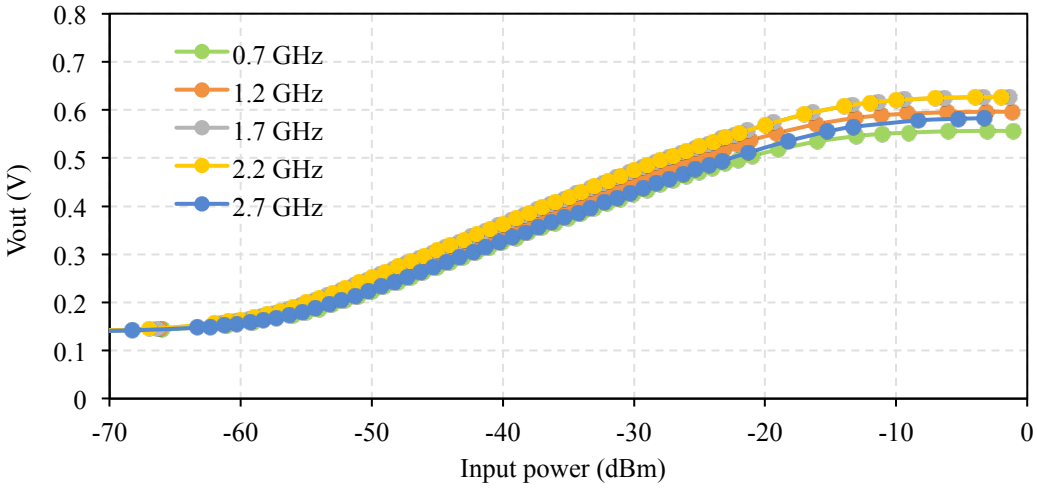



(a)

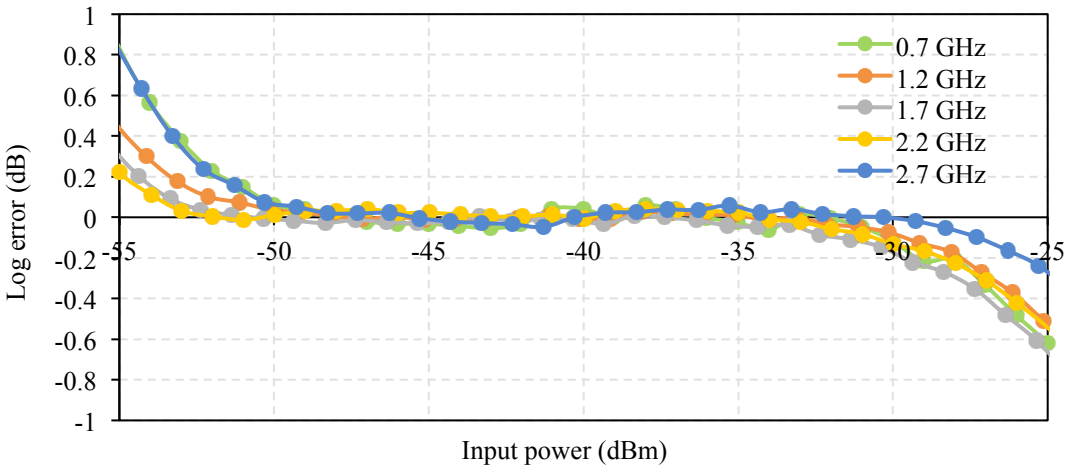

(b)

**Figure 4.5** The fabricated logarithmic amplifier (a) Die photograph and (b) The test board

Selected measured results are shown in Figure 4.6 and 4.7. Figure 4.6 (a) shows the measured input-output curve at several different frequencies. Because of the digital calibration, the curves in Figure 4.6 (a) are quite similar each other. The computed log error, plotted in Figure 4.6 (b) is less than ± 0.06 dB over input dynamic range of 20 dB at the frequency from 0.7 GHz to 2.7 GHz.




(a)




(b)

**Figure 4.6** Measured results (a) Transfer curves of logarithmic amplifier at different frequencies and (b) The computed log errors

Video BW was measured as well while applying amplitude modulated signals having a modulation index of 0.1. As shown in Figure, measured video BW is larger than 175 MHz at all operating condition, which exceed the previously determined target, 60 MHz.

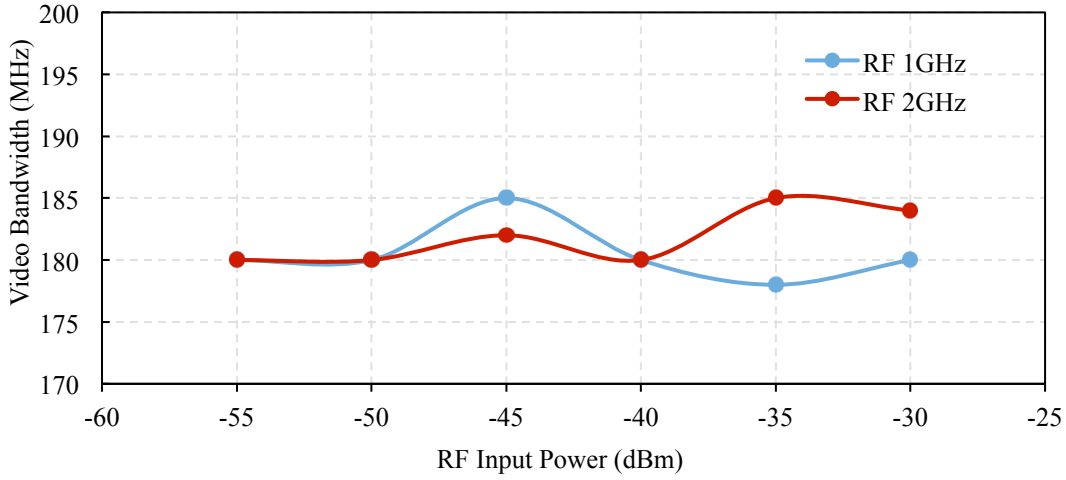



**Figure 4.7** Measured video bandwidth at RF frequency of 1 GHz and 2 GHz

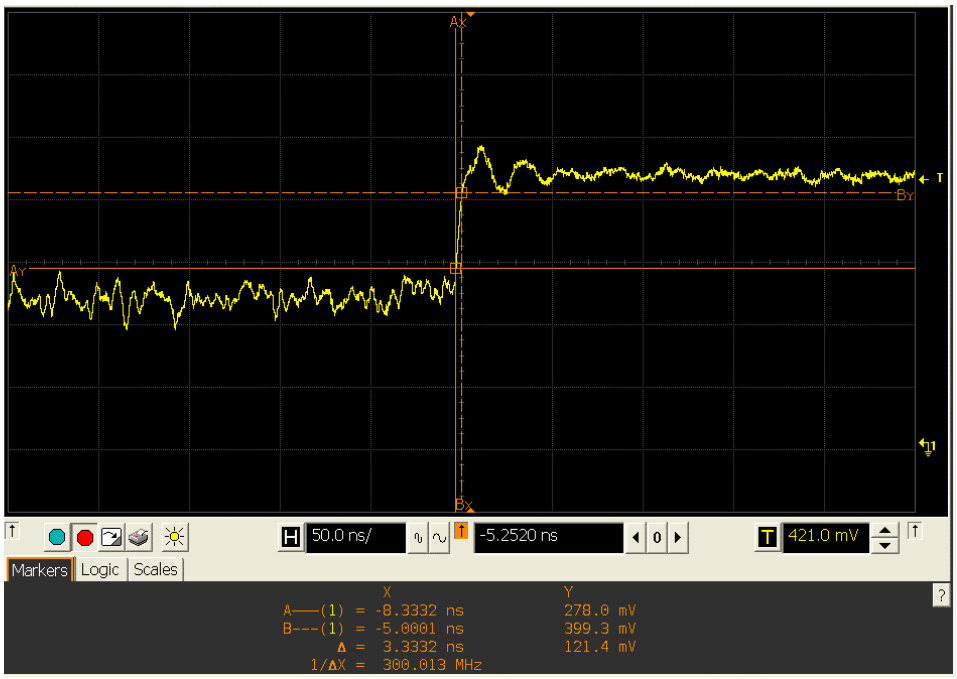



**Figure 4.8** The oscilloscope screenshot captured to measure the response time of log amp

Rise time was measured using oscilloscope, Agilent MSO8104A. An RF input was stepped from -50 dBm to -30 dBm, and the output of log detector was observed. Figure 4.8 is the screen shot that was taken from the oscilloscope. From this measured rise time, the effects of oscilloscope BW and prove BW were excluded. As a result, measured rise time of the log amp is 2.8 ns.

Table 4.3 summarizes the overall performance of log amp. These measurement results exceeded conventional log amp performance in several areas, thus allowing its use in APD systems.

**Table 4.3** Measured performance summary of the logarithmic amplifier

| **Quantity** | **Target** | **Measured data** |
|---|---|---|
| Supply current | | 8.25 mA |
| Power | | 14.85 mW |
| RF operating frequency | 0.7 – 2.7 GHz | 0.7 – 2.7 GHz |
| Input dynamic range | > 20 dB | 24 dB at 2 GHz RF input<br>(Worst case 19.5 dB at 0.7 GHz) |
| Log error within input dynamic range of 20 dB | < ± 0.5 dB | ≤ ± 0.15 dB |
| Response time | < 3 ns | 2.3 ns |
| Video bandwidth | > 60 MHz | 178 MHz |

## 4.4 Circuit Designs of the Phase Detector

### 4.4.1 Architecture of the Phase Detector

Based on the required specifications in Table 4.1, a phase detector was designed, and it consists of three stages: limiters, a Gilbert cell [54], and a low-pass filter (LPF).

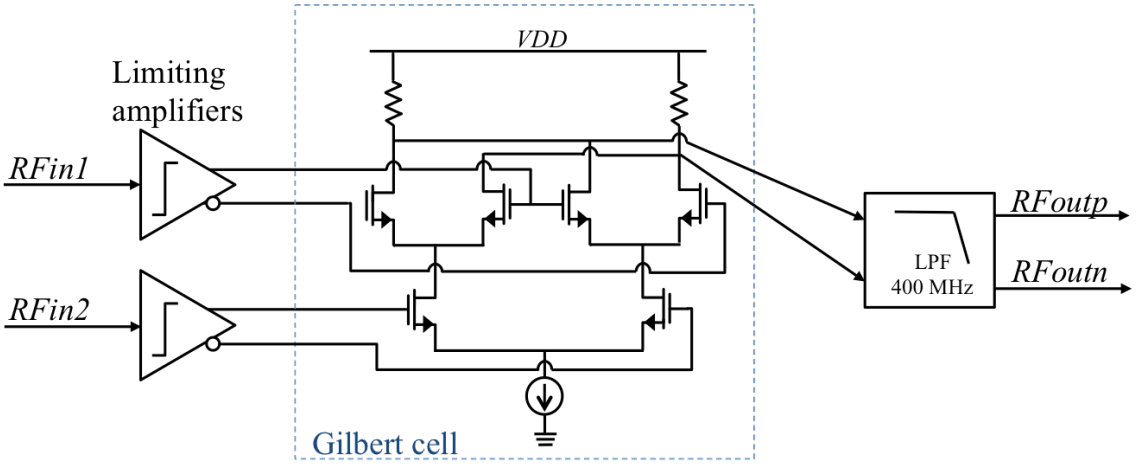
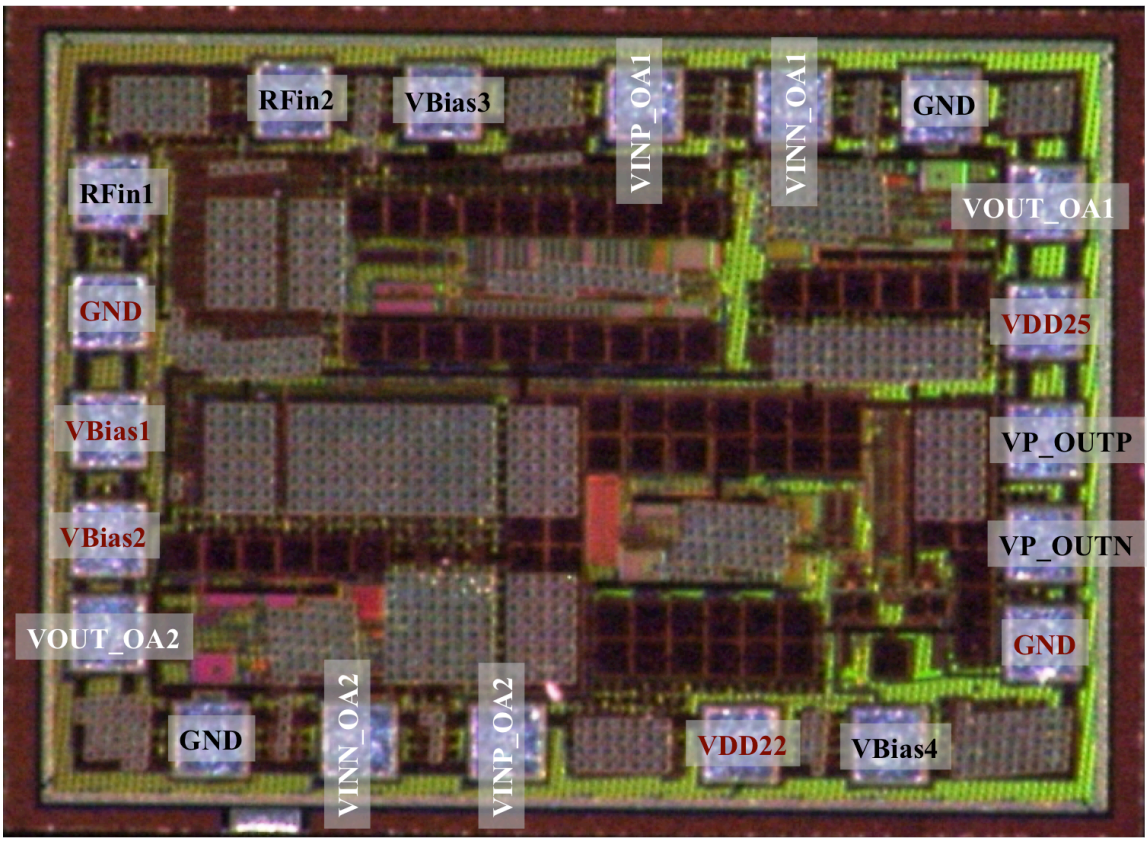


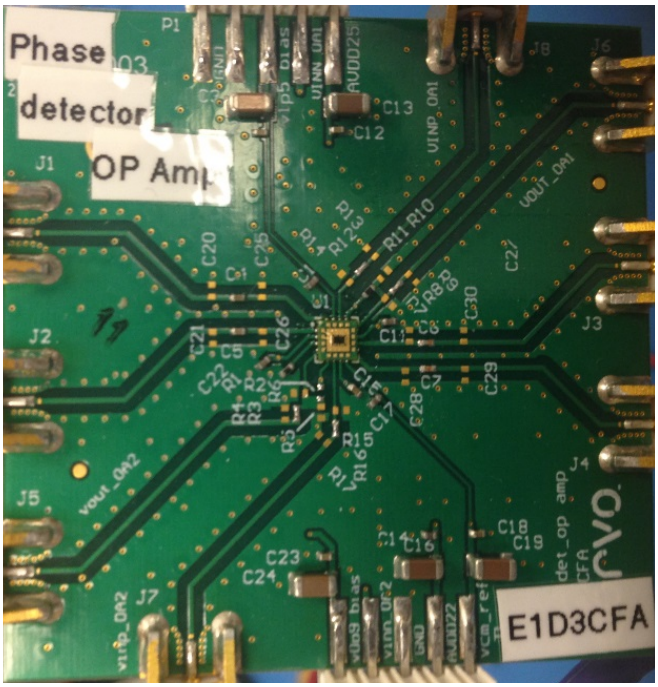

**Figure 4.9** Block diagram of the phase detector for use in APD applications

Limiting amplifiers, a first stage of a phase detector, have two roles. First, these limiting amplifiers change a single-ended input to a differential signal. Second, since the output of a Gilbert cell is a function of the amplitude of the two inputs as well as the relative phase between two inputs, the limiting amplifiers should provide constant amplitude signals to the Gilbert cell by saturating them, making the output of the gilbert cell a function of only the relative phase between RFin1 and RFin2. An LPF is placed at the output of the Gilbert cell so that the LPF removes the high-frequency product generated by the Gilbert cell. The cut-off frequency of LPF was carefully chosen so as not to increase its group delay by more than 2 ns.

### 4.4.2 Measured Results of the Phase Detector




(a)




(b)

**Figure 4.10** The fabricated phase detector and two op-amps (a) Die photograph and (b) The test board

The phase detector and two operational amplifiers (op-amps) are included fabricated together in a single die. The more detail information of the op-amps will be presented in the later section. The die photograph is shown in Figure 4.10 (a). Pin names colored in black, white, and red represent the pins of the phase detector, op-amps, and common pins of both phase detector and op-amps, respectively. This die was packaged and mounted on a PCB for test purposes as shown in Figure 4.10 (b).

Two different RF signals with 10 kHz different frequencies (0.8 GHz and 0.80001 GHz) were applied to two inputs pin of the fabricated phase detector. The output of the phase detector was observed by oscilloscope, Agilent MSO8104A. Captured screen from the oscilloscope is shown in Figure 4.11.

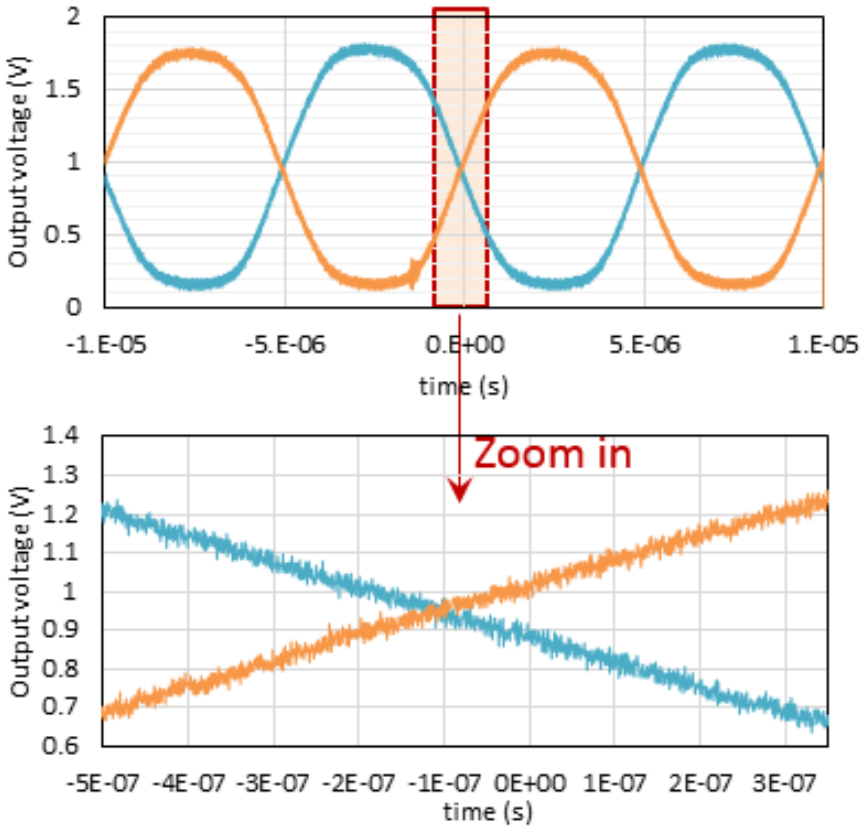



**Figure 4.11** Measured output of the phase detector when 0.8 GHz and 0.80001 GHz RF inputs were applied to the phase detector

Output voltage of the phase detector is linear so that the line in Figure 4.11 is very straight at the region of the relative phase difference of two inputs from 75° to 105°. If this region is utilized in APD systems, then this phase detector can detect AM-PM error accurately.

When the input power of the phase detector gets lower than a certain threshold, liming amplifiers in the phase detector begins to be not able to deliver saturated RF signals to gilbert cell, and the phase detector does not produce valid outputs. Input power was swept from -40 dBm to 10 dBm, and the amplitudes of the phase detector output were measured. Relative amplitudes when compared to the amplitude of valid output at that frequency are plotted in Figure 4.12.

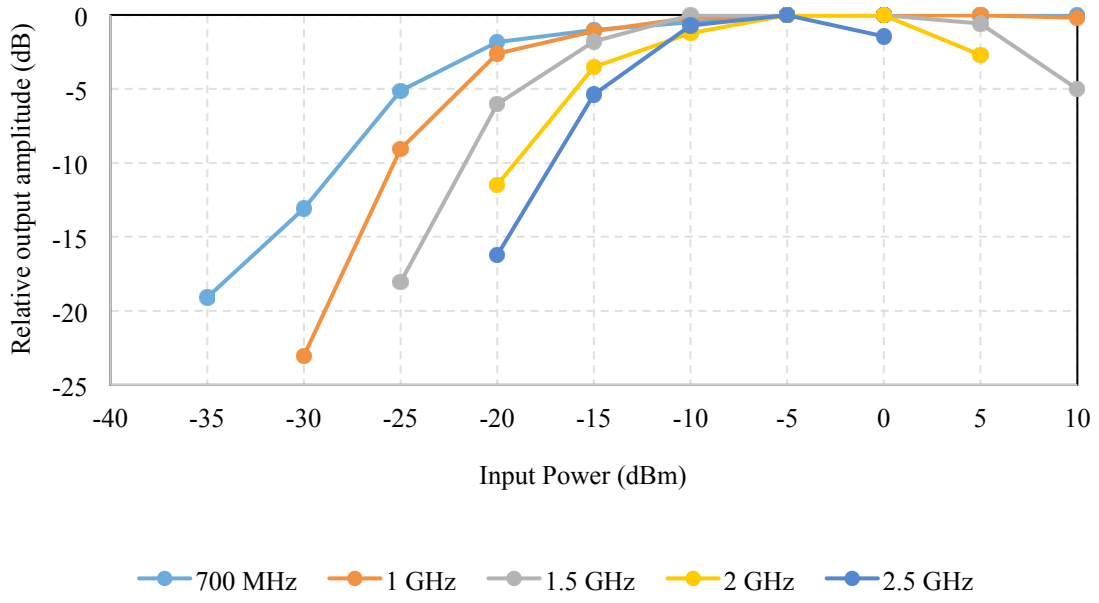



**Figure 4.12** Measured input dynamic range at different frequencies

At a 700 MHz frequency, the input power range of the phase detector is the power larger than -25 dBm. However, the poles at the limiting amplifiers makes the gain of the limitng amplifiers roll off, and starts to increase the lowest power within the input dynamic range of the phase detector. At a frequency of 2.5 GHz, highest power within the input dynamic range is 0 dBm because the output stage in the LPF starts to distort the signals at the high input power.

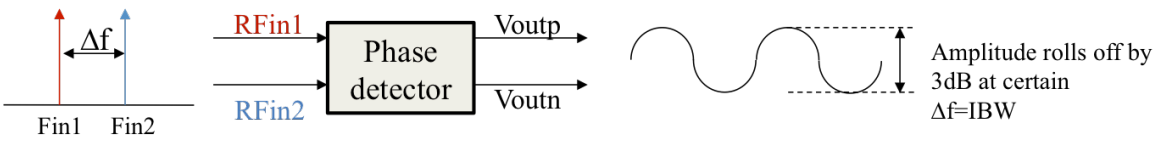



**Figure 4.13** Test setting to measure instantaneous bandwidth

Figure 4.13 shows the test setting to measure an instantaneous bandwidth (IBW) of the phase detector. A two-tone signals with a very small frequency difference was applied to phase detector and the amplitude of the output voltage was measured. As the frequency difference between a two-tone signals increases, the output voltage drops by 3dB at some point. This frequency difference is the IBW, which is shown in Figure 4.14.

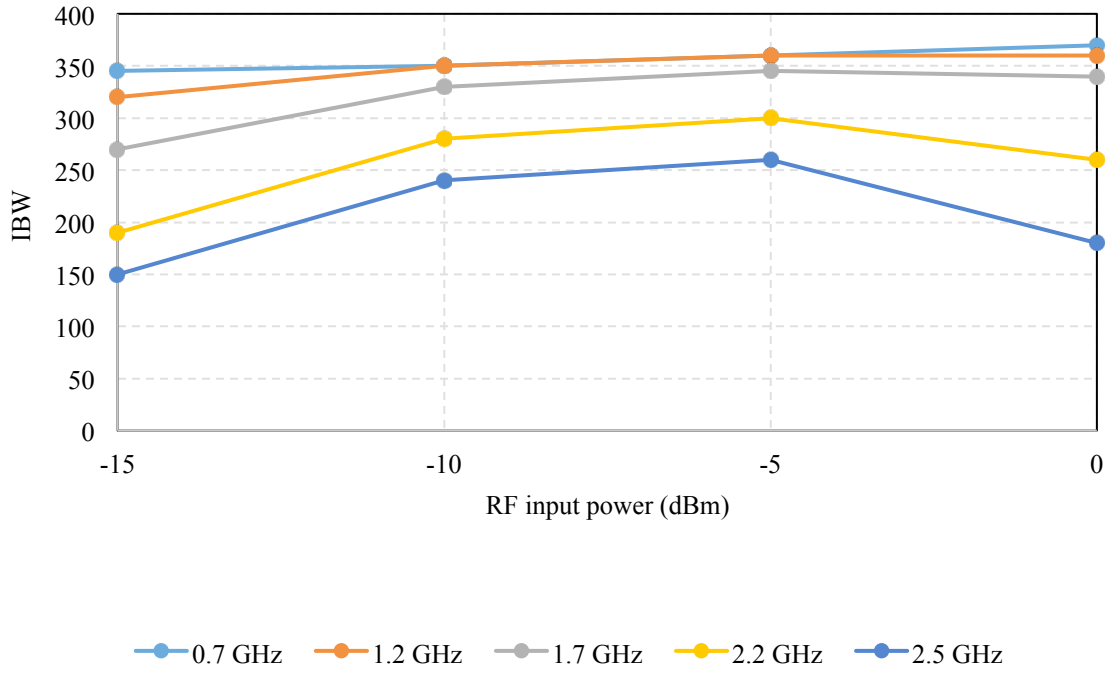



**Figure 4.14** Measured instantaneous bandwidth at different frequencies

Measured IBWs are over 150 MHz at all operating conditions, which means that this phase detector can detects AM-PM errors in PAs that is less than 150 MHz. Below Table 4.4 summarizes the measurement of the phase detector, which proves that this phase detector will be able to accurately detect AM-PM errors less than 30° in an RF signal with a channel BW of 30 MHz.

Table 4.4 Measured performance of the phase detector

| **Quantity** | **Target** | **Measured data** |
|---|---|---|
| Power<br>(includes power of two op-amps) | | 42.05 mW |
| RF operating frequency | 0.7 – 2.7 GHz | 0.7 – 2.7 GHz |
| Input dynamic range | | RF 700 MHz: Pin >-25 dBm<br>RF 2.5 GHz: -12 dBm<Pin< 0dBm |
| Input phase differential range for linear detection | 30° | 30° ($75^{o} < \Delta\varphi < 105^{o}$) |
| IBW | > 100 MHz | 150 MHz |

# CHAPTER 5

# ANALOG PREDISTORTION SYSTEM DESIGNS

## 5.1 Introduction

In this work, the analog predistortion (APD) system for improving PA linearity will be proposed. An APD system is built by assembling the analog circuits designed in previous chapters such as the VPS, the VGA, and the log amp on a PCB. First, system simulations using ADS have been done using the behavior models of a PA, designed VPS, VGA, and log amp. Issues that might become problems in the process of realizing the system on a PCB will be addressed, and solutions will be presented accordingly. From these design considerations, the APD test board has built, and measurements have been taken on this board. Lastly, measured data and simulation results will be compared and discussed to conclude this chapter.

## 5.2 Design Considerations in APD System Designs

Figure 5.1 shows the APD system design with several more considerations that take into account. Blue-colored blocks are the fabricated circuits that were designed for use in APD applications at the previous chapters, such as the VPS, the VGA, the log amp and the phase detector. While developing the board-level APD system using these components, it has been discovered that three issues need to be addressed. These problems will be explained and what care has been taken to resolve them will be presented.

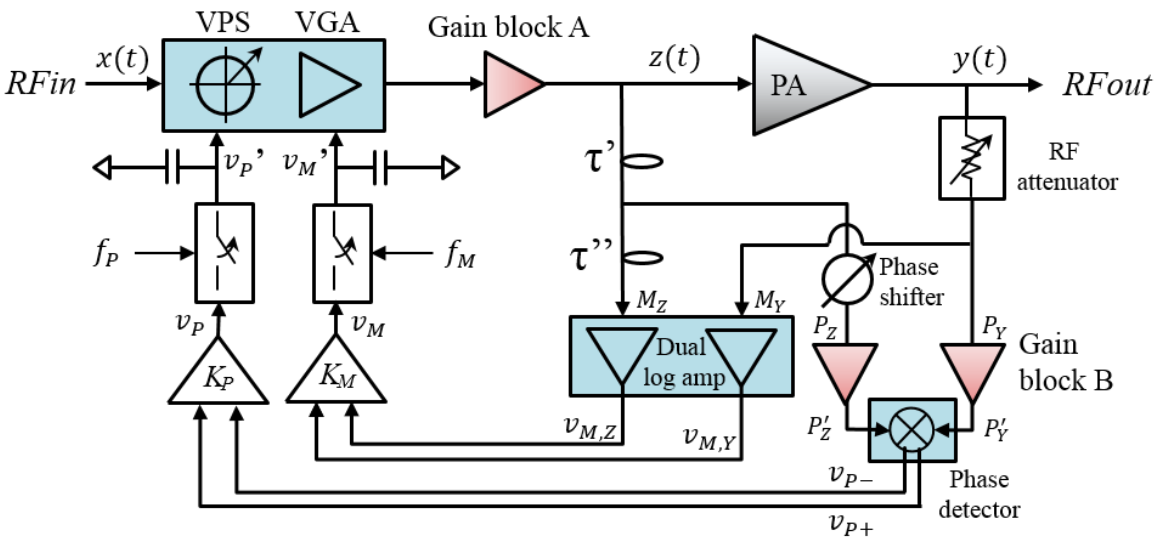



**Figure 5.1** Block diagram of proposed APD system

### 5.2.1 Tunable and Reconfigurable Delay Line

The two inputs to the log amp, $M_A$ and $M_B$, need to be matched to compare the amplitudes of input and output of PA exactly and extract the AM-AM errors of PA. Likewise, the two inputs to the phase detector, $P_A$ and $P_B$, have to be matched. Two delay lines, $\tau'$and $\tau''$ are inserted as illustrated in Figure 5.1. A delay line of $\tau'$ is used to equalize the delays of two input to the phase detector, and a delay line of $\tau''$ matches the delays between two inputs to the dual log amp. These delay lines were designed to be reconfigurable and tunable.

First of all, as shown in Figure 5.1, using different combinations of two different power combiner/splitters having two different delays (400 ps, 10 ps) are utilized to increase or decrease coarsely the delay of 400 ps. Also, when a delay of more than 2 ns is needed, then a 2 ns delay line from Anaren will be inserted.

Secondly, to finely control the delay in the delay lines, true time delay (TTD) lines using inductors and varactors were designed. By controlling the cathode voltage of varactors, the amount of delay is precisely controllable. The delay per LC stage can be calculated as shown in (5.1). Adjustable range of $C_{var}$ was determined by the range that the TTD did not make the reflection, more than -10 dB, caused by the mismatch between the impedance of TTD and a 50 Ω transmission line.

$$Delay\ per\ stage = \sqrt{LC_{var}} \tag{5.1}$$

$$Impedance\ of\ TTD = \sqrt{\frac{L}{C_{var}}} \tag{5.2}$$

An RF switch (SP6T) determines the number of TTD stages. The inductance of the inductor, controllable capacitance ranges of varactors and the required number of TTD stages were carefully chosen by computer simulations so that they cover the enough RF BW, and the amount of controllable delay.

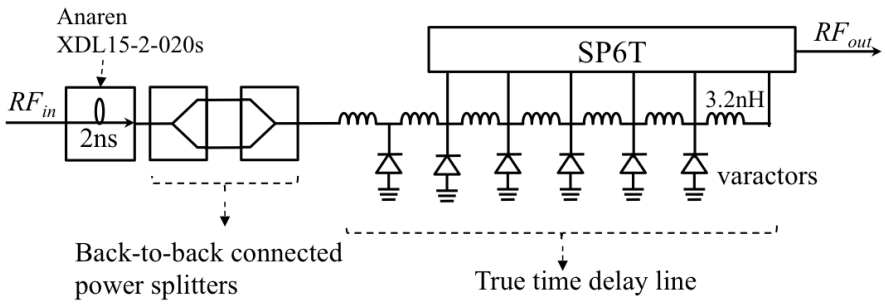



**Figure 5.2** Reconfigurable and tunable delay line design

This TTD was built on a PCB by mounting a Skyworks varactor (SMV1247) and inductors. It was tested, and the measured results are shown in Figure 5.3. When

sweeping the cathode voltage of SMV1247 from 2.5 V to 5 V, this TTD showed a delay control of 300 ps while still keeping the 5 dB loss at this TTD.

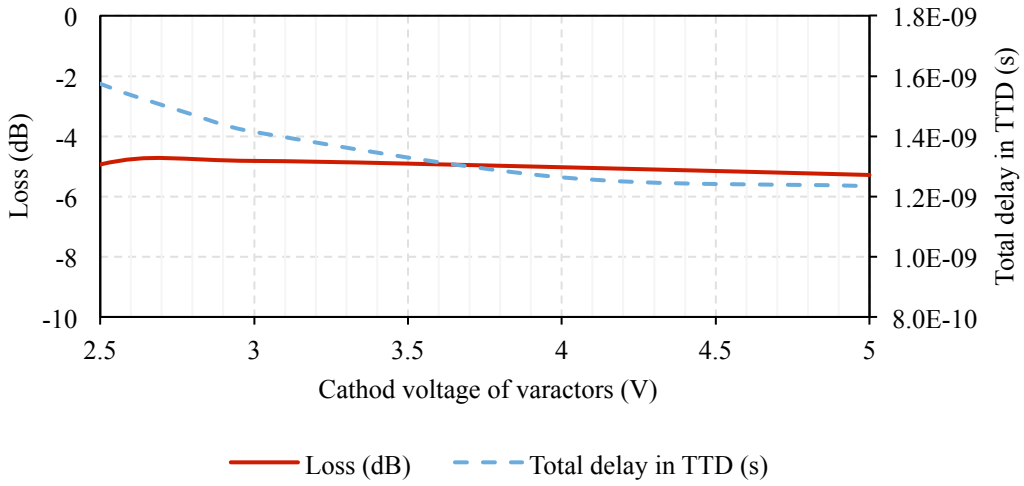



**Figure 5.3** Measured delay and loss of the true-time delay device

### 5.2.2 Mechanism of Freezing Loop

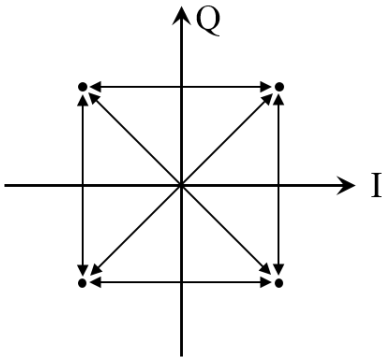



**Figure 5.4** QPSK constellation

Figure 5.4 shows the QPSK signal constellation and phase transition between each symbol. When the phase transition of 180° occurs, then the signal trajectory passes

through the origin, which is called as a zero crossing. This zero crossing happens at 16 QAM and 64 QAM as well. Every time a zero crossing is encountered, the amplitude of RF signal drops to zero. The input power to the log amps and the phase detector in APD system gets lower than the effective input power range, then the log amps and the phase detector will produce invalid outputs, making the APD system unstable. Thus, there has to be a way to hold or freeze the APD systems when the RF power gets lower than certain thresholds.

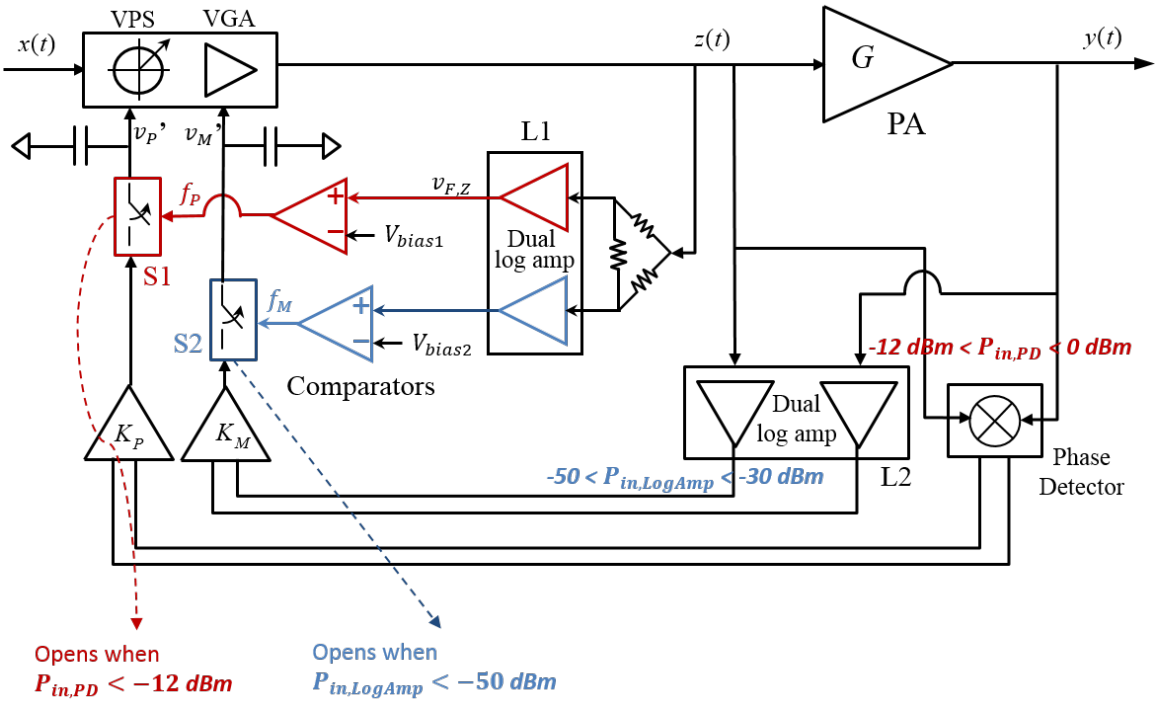
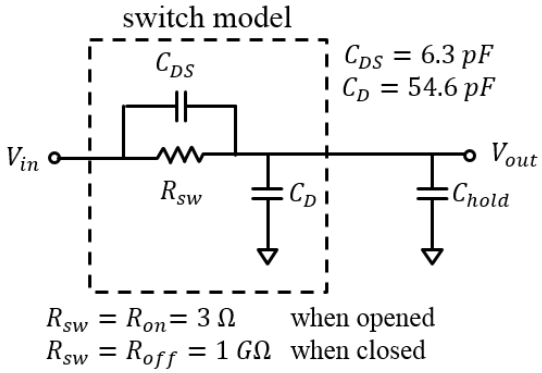


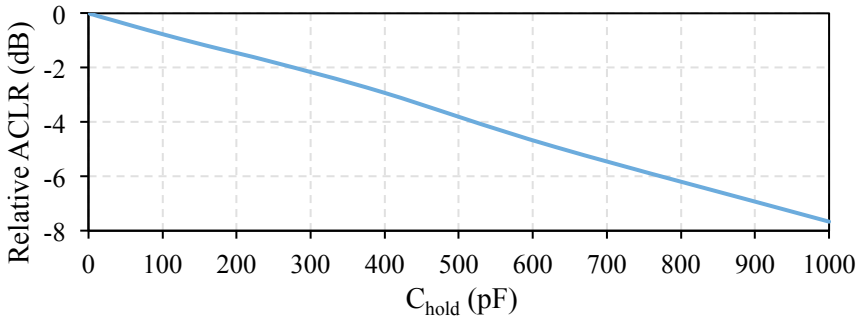

**Figure 5.5** Block diagram of the proposed APD that shows the freezing loop exclusively

Two analog switches, S1 and S2, are placed between $K_P$ and the VPS control pin, and between $K_M$ and the VGA control pin, respectively. The PA input, z(t), is splitted into two paths by a resistive power divider and goes to L1 to detect a power. Outputs of L1 are compared to the bias voltage to decide if the power of z(t) is lower than the

effective input dynamic range of L2 or the phase detector. If so, $f_M$ and $f_P$ signal coming from L1 will open the switches, and capacitors between the control ports of VPS and VGA and switches hold the voltage while switches open. The capacitances of these capacitor must be chosen carefully because a larger capacitance will more likely hold the voltages but limit the loop bandwidth, degrading APD performances. To decide the appropriate capacitance, the capacitances were slept from 0.1 pF to 100 pF while measuring ACPR improvements in ADS simulations. A simulation model of analog switch (TS3DS26227) was built based on its datasheet [55]. The following Figure 5.6 (a) shows the switch model used in simulations with the hold capacitor at the output of the switch.




(a)




(b)

**Figure 5.6** Analog switch design (a) Model used in simulations (b) Effects of the capacitance of the hold capacitor to APD performances

The APD was simulated with various capacitances of $C_{hold}$ and compared to the ACPR got with $C_{hold}$ = 0 pF. Relative ACPR is the difference between maximum ACPR, which is gotten with $C_{hold}$ = 0 pF, and ACPR with various $C_{hold}$, as following Equation 5.3.

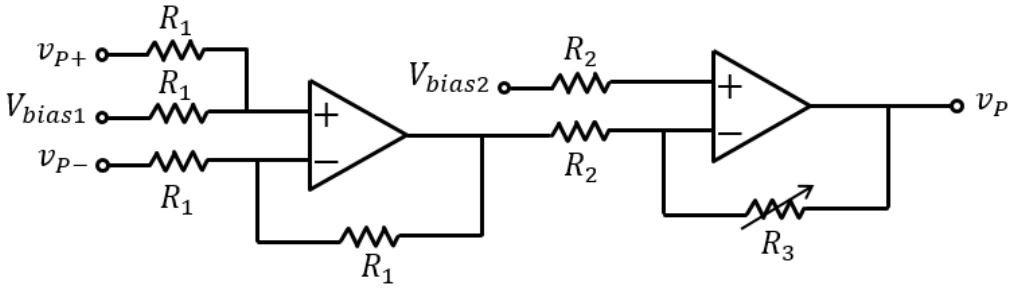
$$Relative\ ACPR\ (dB) = ACPR(C_{hold} = 0\ pF) - ACPR(C_{hold}) \tag{5.3}$$

The capacitance of $C_{hold}$ was selected as 10 pF to minimize the ACPR degradation, but this value is large enough to hold the final value right before switch opening.

### 5.2.3 Interface Circuit Design

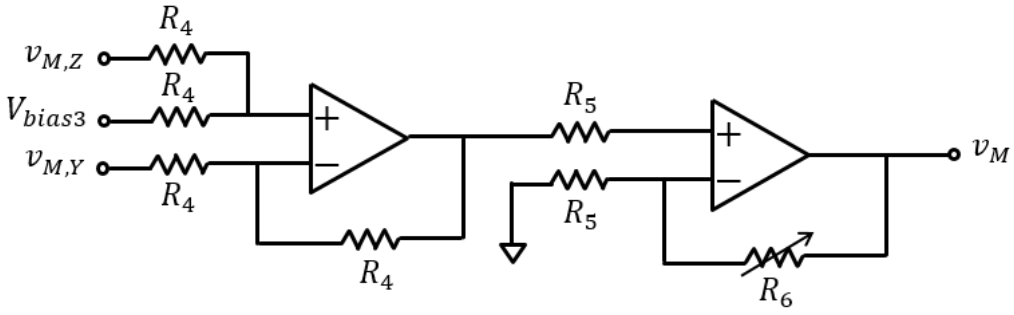
#### *5.2.3.1 Loop circuitries*

The interface blocks, $K_P$ and $K_M$ in Figure 5.1, are designed using the operational amplifier (op-amp) to reduce the discrepancy in the level of the control signal between the PA error detectors (phase detector and log amps) and the signal predistorter (the VPS and the VGA).




$$v_p = -\frac{R_3}{R_2}(v_P^+ - v_P^-) + V_{bias2}\left(1 + \frac{R_3}{R_2}\right) + V_{bias1}\left(\frac{R_3}{R_2}\right)$$

(a)




$$v_M = \left(1 + \frac{R_6}{R_5}\right)(v_{M,Z} - v_{M,Y}) + V_{bias3}\left(1 + \frac{R_6}{R_5}\right)$$

(b)

**Figure 5.7** Loop circuitries (a) Phase control loop circuitry between VPS control pin and phase detector (b) Magnitude control loop circuitry between VGA control pin and log detectors.

An op-amp for use in above loop circuitries in Figure 5.7 has to be fast enough to deliver the detected AM-AM or AM-PM errors in PAs to PA predistorters. Through computer simulations, it has been determined that the gain-bandwidth product of an op-amp needs to be larger than 500 MHz, and the op-amp has to operate in a stable condition, even with a closed-loop gain of 0 dB.

The topology chosen for this op-amp design was a two-stage cascode amplifier to provide enough bandwidth and a high gain, as illustrated in Figure 5.8. Rail-to-rail input and output were utilized in this design to enable both input and output to go alsmost as low as ground and as high as a supply voltage.

As shown in Figure 4.10, the op-amp was fabricated with the phase detector in a single die, utilizing a 0.18 um SiGe BiCMOS process.

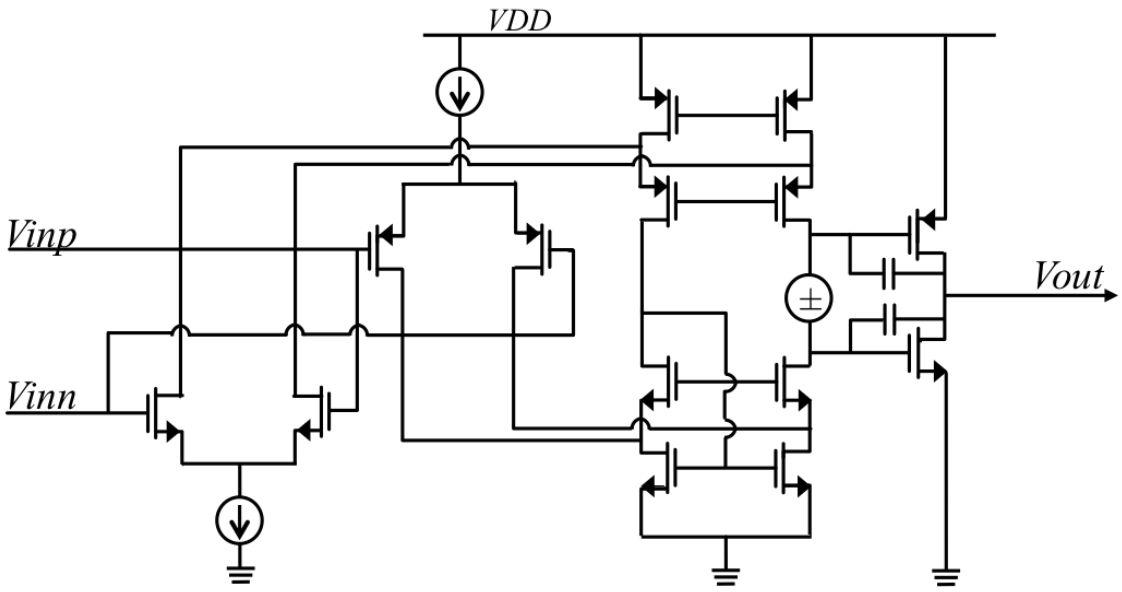



**Figure 5.8** Schematic of the operation amplifier for use in the loop circuitries of APD systems

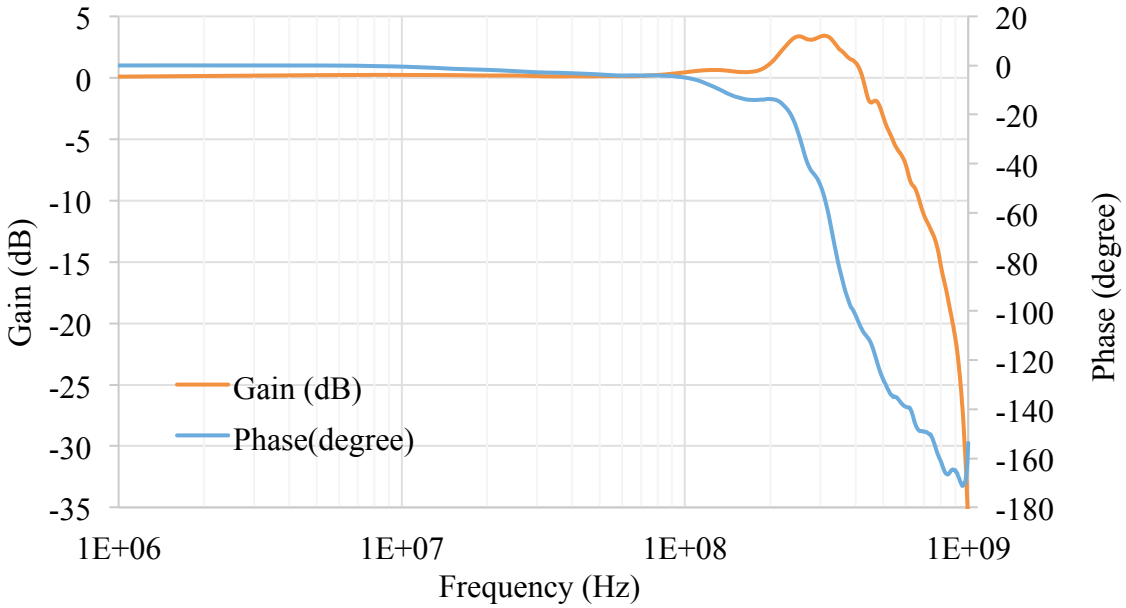


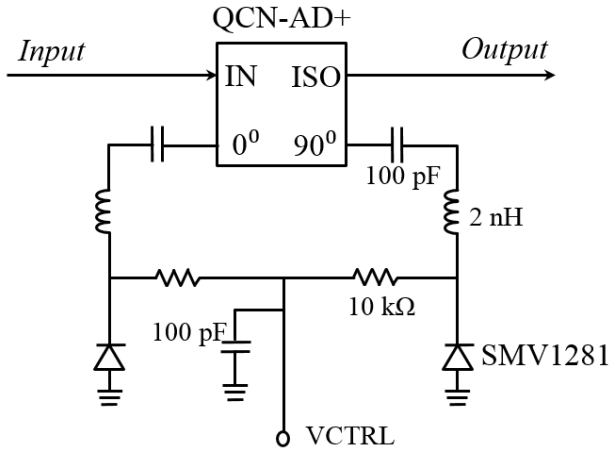

**Figure 5.9** Measured gain and phase response of op-amp that is in unity-gain configuration.

The inverting input pin was connected to the output pin of the op-amp, and then the gain and phase of the op-amp were measured by the network analyzer, Agilent 5071C, as shown in Figure 5.9.

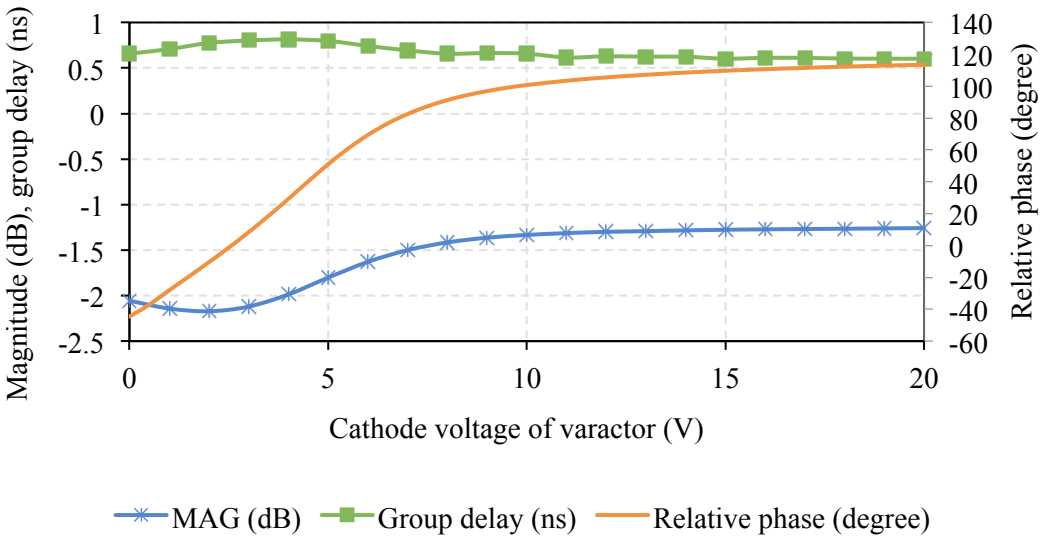
Because of the 50-Ω loading from the network analyzer, the measured bandwidth was 496 MHz with a phase margin of 50°. Since the op-amp will be used in high-impedance loading environments, this op-amp will operate with a higher bandwidth and a better phase margin.

### *5.2.3.2 Reflection-type Phase Shifter Design*

Also, when there's no AM-PM error in a PA, then the phases of the two inputs, $P_Z$ and $P_Y$ to the phase detector in the APD system must have exactly a 90◦ difference. Therefore, reflection-type phase shifter using a 90◦ hybrid coupler (Mini-circuits QCN-12AD+), SMD inductors, and varactors (Skyworks SMV1281) [56] is designed as Figure 5.10 (a).




(a)




(b)

**Figure 5.10** Reflection-type phase shifter using a 90◦ hybrid coupler (a) Phase control loop circuitry between VPS control pin and phase detector (b) Measured responses over the control voltage at 881.5 MHz

This phase shifter was built on PCB board for a test purpose. Magnitude response between the input and the output, the group delay, and the phase shift with the voltage of the cathode of varactor were measured, and these results are shown in Figure 5.10 (b). This designed phase shifter shows a total phase shifting range of 150° with a delay of 0.7 ns ~ 1 ns and a loss of 2 dB.

### 5.2.4 Gain Blocks

Qorvo RFPA0875 produces a maximum output power of 28 dBm when the power of an input signal is -1 dBm. To make the APD systems in Figure 5.1 work, the circuit that has VPS and VGA needs to deliver RF power of at least -1 dBm to the PA input. However, the measured IP1dB of cascaded VPS and VGA in the previous chapter is -18.44 dBm at RF 1 GHz, which means that this designed VPS and VGA must be driven

at back-off from this IP1dB not to introduce the nonlinearities of this circuit. Gain block A in Figure 5.1 is used to remove the discrepancy of required input power to PA and capable of driven power of the cascaded VPS and VGA circuit.

However, this gain block A amplifies the noise generated in cascaded VPS and VGA circuit and generates its own additional noise, degrading the performance of the APD system. Therefore, the amount of gain of a gain block needs to be adjusted (1) to be large enough that the circuit of VPS and VGA operates at sufficiently backed-off mode so that VPS and VGA do not introduce its nonlinearity, (2) to be not too large so that this gain block does not make the whole system noisy. If the system becomes too noisy, then noise floor at the output of the APD system will be higher than the sidebands of the RF main channel so that it is impossible to see any ACPR improvements with the APD.

To see the effects of the NF of the gain block A, computer simulations have been conducted. The behavior models of each circuit were used based on the measured results and it was assumed that there were no noise contributions from circuits other than the gain block A. LTE signals with several different channel bandwidths, 2 MHz, 5 MHz, 10 MHz, and 20 MHz, were applied, and ACPR at the output of the system were calculated in the simulations. The results from these simulations are plotted in Figure 5.11.

First of all, the NF of the gain block A were set to 0 dB, and ACPRs when APD is on and off were compared. When APD is off, ACPR is not a function of channel bandwidth, as shown in the orange line in Figure 5.11. When APD is on (blue line in Figure 5.11), ACPR improvement decreases as the BW increases because of the loop delay in APD system.

On the other hand, when the gain block A has the NF of 3dB, then ACPR, when the APD is off, becomes a function of the channel bandwidth. In other words, ACPR degrades as channel bandwidth increases, as illustrated in the yellow line in Figure 5.11. Furthermore, when APD is on, ACPR improvements are degraded in APD system with a wider channel BW. ACPR improvement is nearly negligible, with the signal having the channel bandwidth of 20 MHz. For this reason, NF of the gain block A has to be as low as possible to ensure the correction of the signal that has a wide channel bandwidth. Through excessive simulations, Qorvo QPA4563A, that exhibits the 2.4 dB NF and 25.5 dB gain at 881.5 MHz, has been chosen.

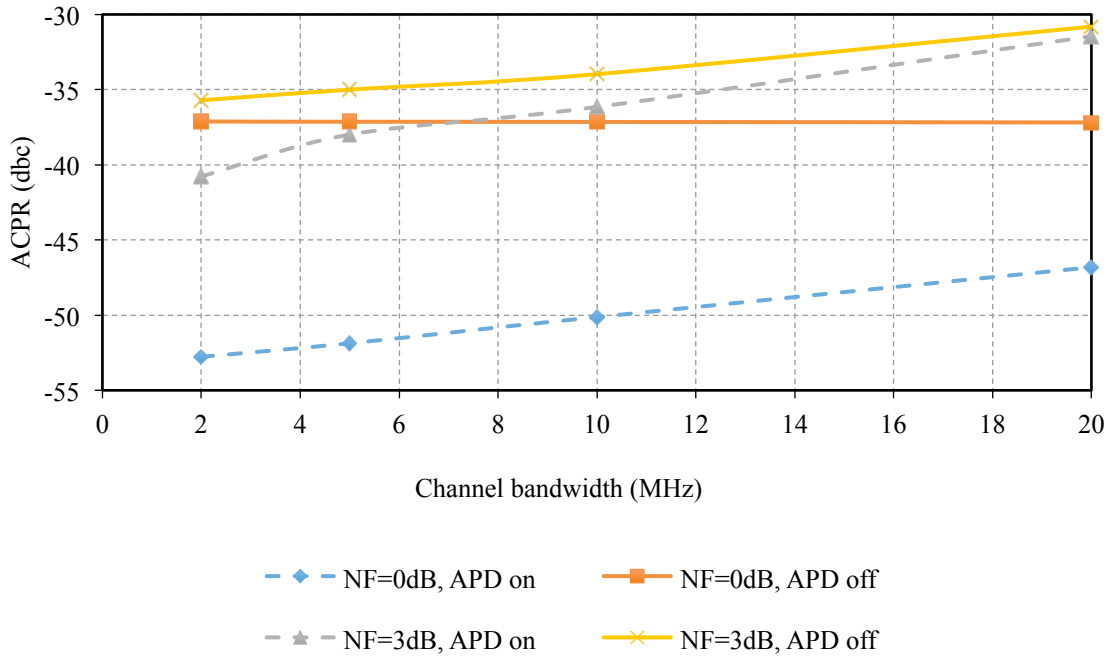



**Figure 5.11** NF effects on the APD systems

Because the input dynamic range of the phase detector in Figure 5.1 is from -12 dBm to 0 dBm, gain blocks are inserted at two inputs of phase detectors (gain blocks B in

Figure 5.1). For this purpose, Qorvo SGA1263, that exhibits -9.5 dBm OP1dB, is chosen because it will saturate the output signal at around -5 dBm. Since the small-signal gain of SGA1263 is 17 dB at 881.5 MHz, it puts the power of $P_Z$ and $P_Y$, within the input dynamic range of the phase detector if their power is larger than -29 dBm.

## 5.3 Simulation Results and Discussions

APD architecture illustrated in Figure 5.1 is simulated in a Keysight ADS by applying LTE signals as the input to this architecture. Based on the measured characteristic of each analog component including VPS, VGA, and log amp, their behavior models for APD system simulation were constructed. A behavioral model for the amplifier under test was extracted from a 0.5 W PA (Qorvo RFPA0875) by fitting the measured AM-AM and AM-PM distortion. Extracted AM-AM and AM-PM distortion is plotted in Figure 5.12. Losses of PCB traces and SMA connector are not excluded from measured data.

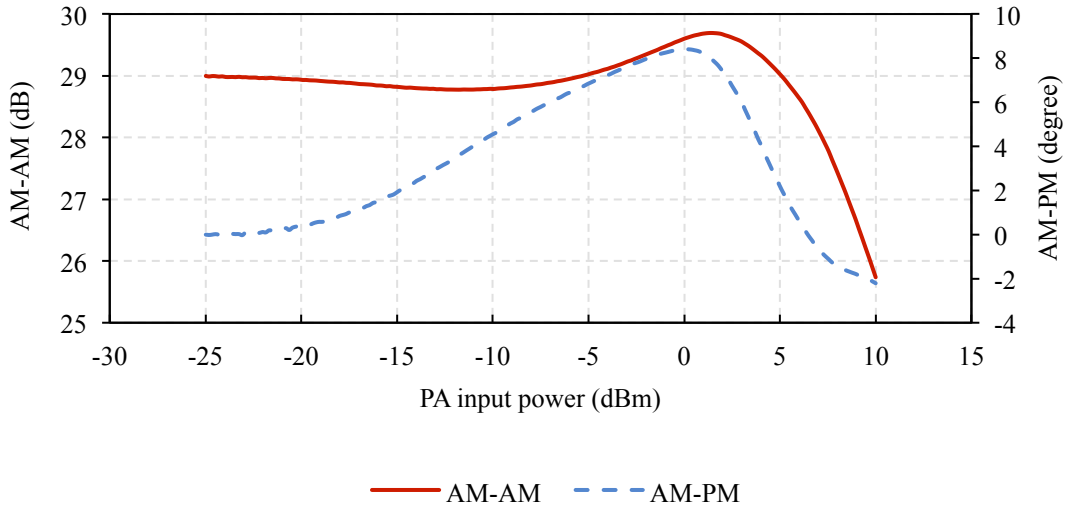



**Figure 5.12** Measured AM-AM and AM-PM distortions in Qorvo RFPA0875

A loop delay of the APD system is the summation of the delay in RFPA0875 and the delay in feedback loop. To see the effects of the loop delay to APD performance exclusively, the loop delay was swept from 0 ns to 20 ns while applying various bandwidth of RF signals. The ACPR1 was measured at the maximum output power (28dBm) that was shown in the datasheet of Qorvo RFPA0875. Figure 5.13 shows the spectrum of PA output in the APD PA linearization system. When assuming the loop delay as 1 ns, an ACPR improvement of 16 dB was achievable for the LTE 20 MHz signal at 28 dBm output power.

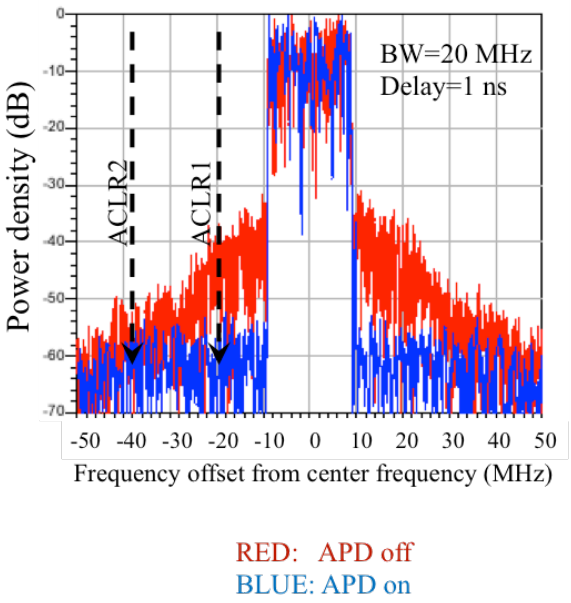



**Figure 5.13** Output spectrum of APD systems in simulations

In Figure 5.14, the ACPR improvements over the loop delay of the APD were investigated. As the loop delay increases, the achievable ACPR improvement gets worse. This tendency is severe with a wider signal BW, which means that the APD system with an RF signal that has wider BW is more vulnerable to the loop delay. For instance, with

the assumption of a 10 ns delay in the loop, ACPR1 correction in an LTE 5 MHz signal drops by a 3 dB, but in an LTE 20 MHz signal it drops by a 12 dB, when compared to the ACPR1 improvement with no loop delay. Therefore, every component on the APD test boards must be closely spaced enough to minimize the loop delay, getting an adequate performance of APD systems even with a wideband signal.

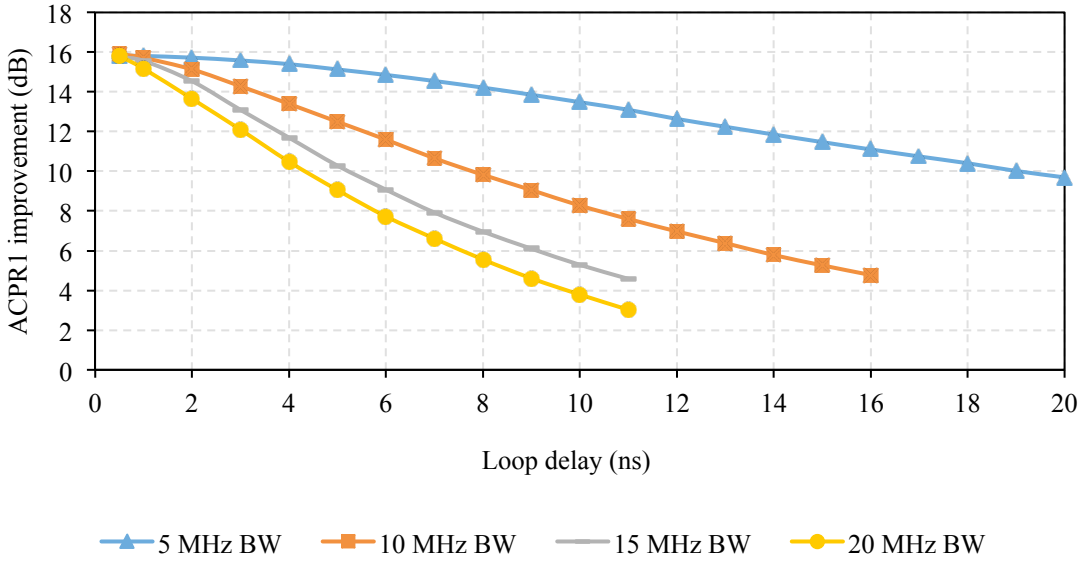



**Figure 5.14** ACPR1 vs. delay (ns) with various bandwidth signal

Another important limitation of this APD technique comes from the inherent group delay of a PA. This group delay cannot be compensated, so that it will eventually limit the performance of the APD even though all of the components in APD systems are super-fast. The measured group delay of Qorvo RFPA0875 is 1.6 ns. Therefore, maximally achievable ACPR1 correction with an LTE 20 MHz is 14 dB, if there's no other delay but PA group delay in this APD system.

## 5.4 Digitally Calibrate-able APD System

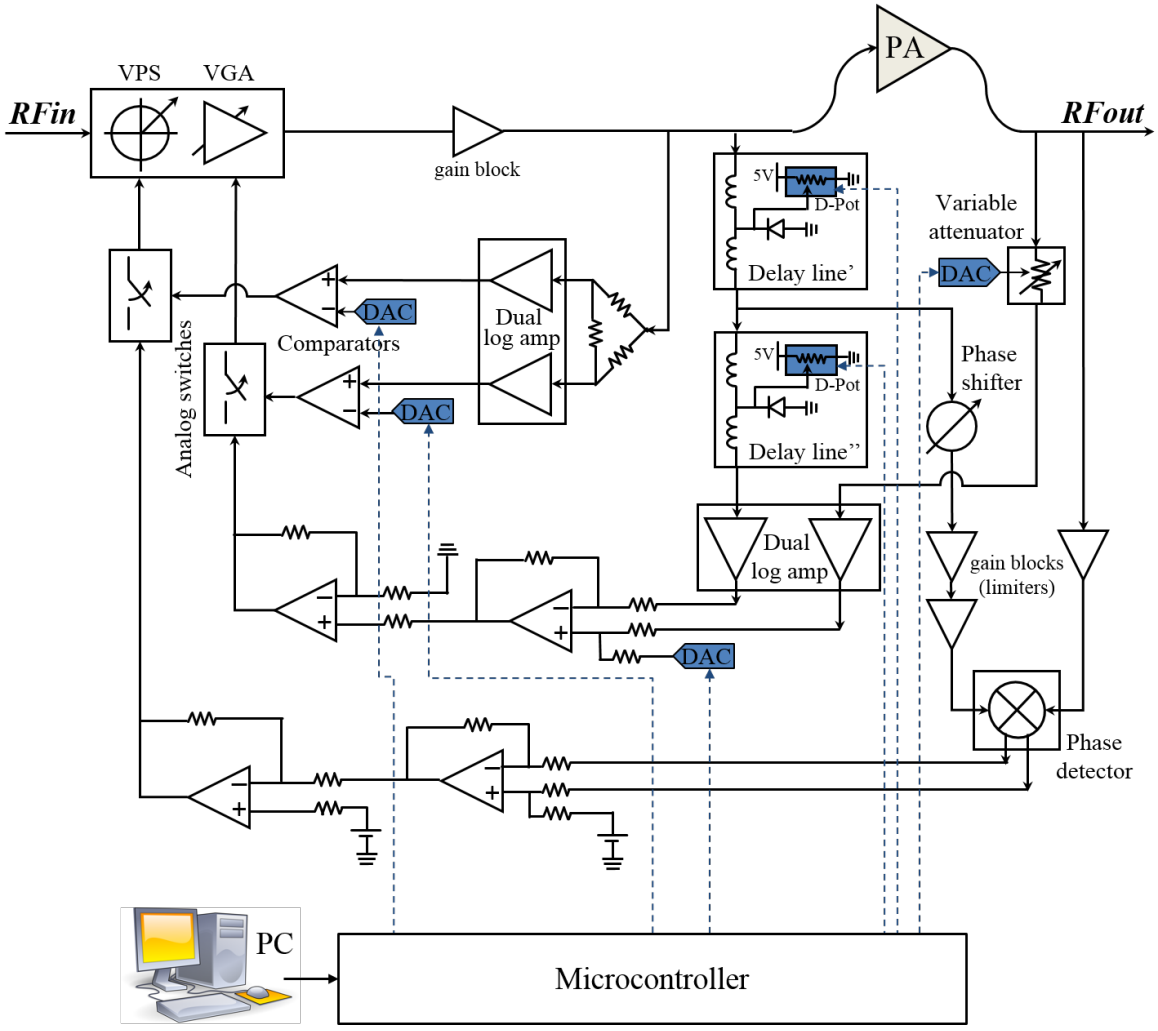



**Figure 5.15** Final schematic of analog predistortion system and a test setup

Analog circuits with a built-in digital calibration capability have appeared in mainstream products because of their superior performances in comparison with conventional analog circuits or systems. Moreover, digital calibration capabilities can help systems find an optimal operating point, which makes analog circuits or systems more robust to unexpected external interferers, process variation, and temperatures.

The calibration circuits for the APD system adopt digital-to-analog converters (DAC), digital potentiometers (digipots), and a microcontroller as shown in Figure 5.15. Digipots in the delay lines are used to adjust a voltage of varactor cathode by controlling the ratio of the resistance between a wiper and one terminal to the resistance between the wiper to the other terminal. Four DACs are used to calibrate the bias voltages that are applied to op-amps and the control voltage of RF attenuators.

Based on the schematic shown in Figure 5.15, the test board was designed and components were mounted on this board as shown in Figure 5.16.

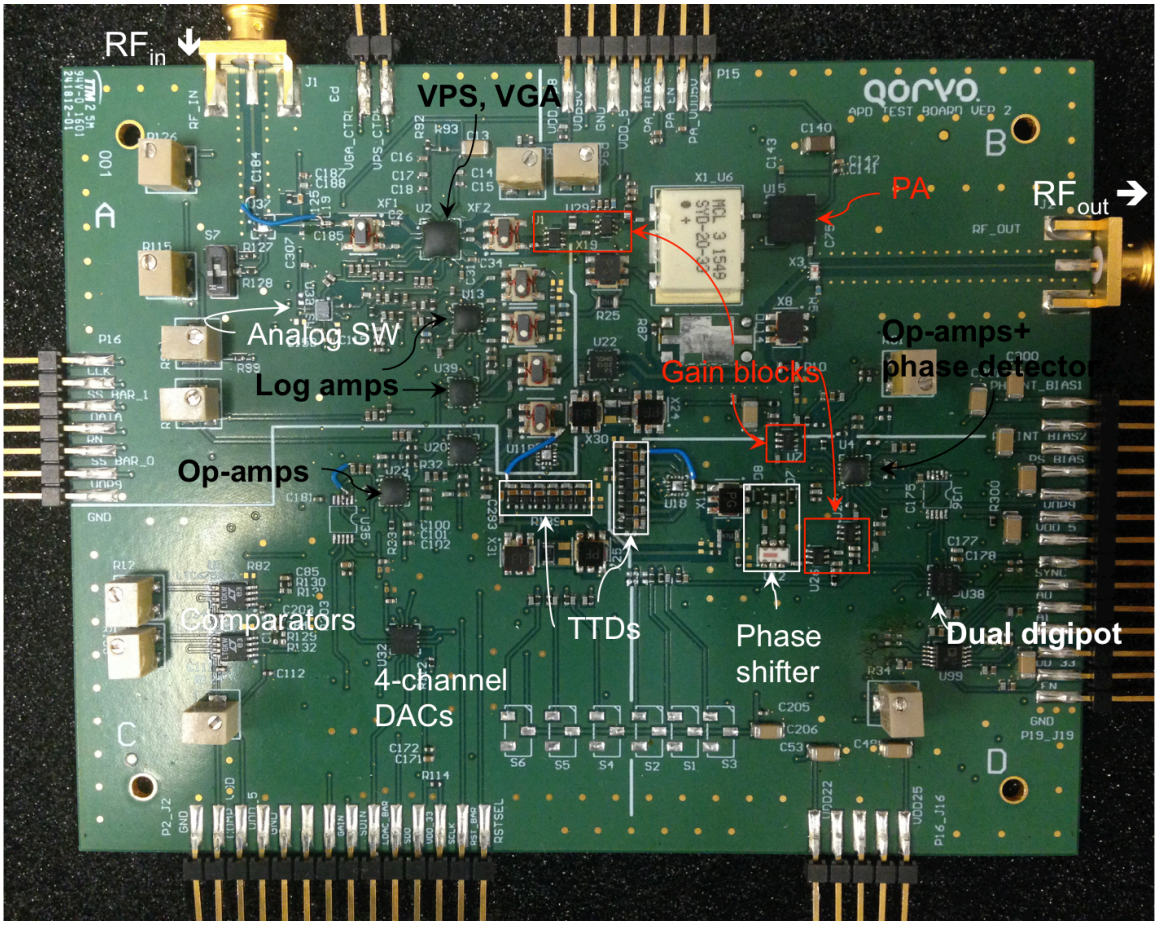
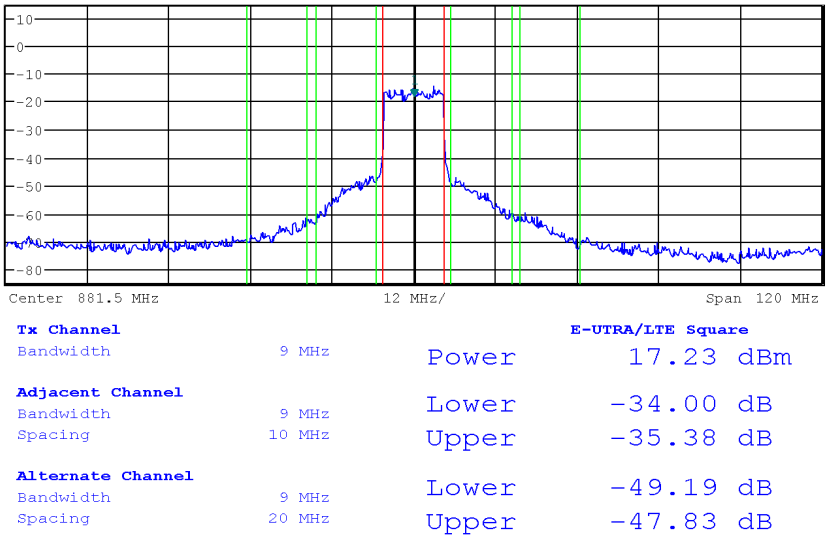


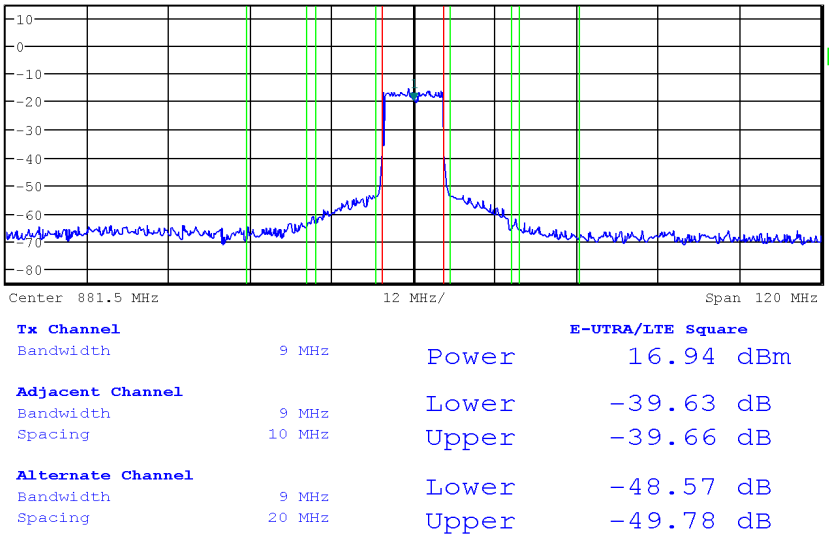

**Figure 5.16** Assembled test board to verify the APD system

## 5.5 Experimental Validations and Discussions

A 10 dB cable attenuator was placed between the spectrum analyzer (R&S FSQ) and the output SMA of the test board to protect the instruments from a power overload. The test board has been calibrated by finding an optimal operating point by sweeping output voltages of the DACs and the resistances of the digital potentiometers.




(a)




(b)

**Figure 5.17** PA output spectrum of the test board with an LTE 10 MHz signal input at output power of 28 dBm (a) APD off (b) APD on

Figure 5.17 shows the spectrum results from the APD performance for LTE 10 MHz signals. There was no improvement of ACPR2, but 5 dB improvement of ACPR1 was achieved at 28 dBm output power for the LTE BW 10 MHz signal having 16QAM modulation.

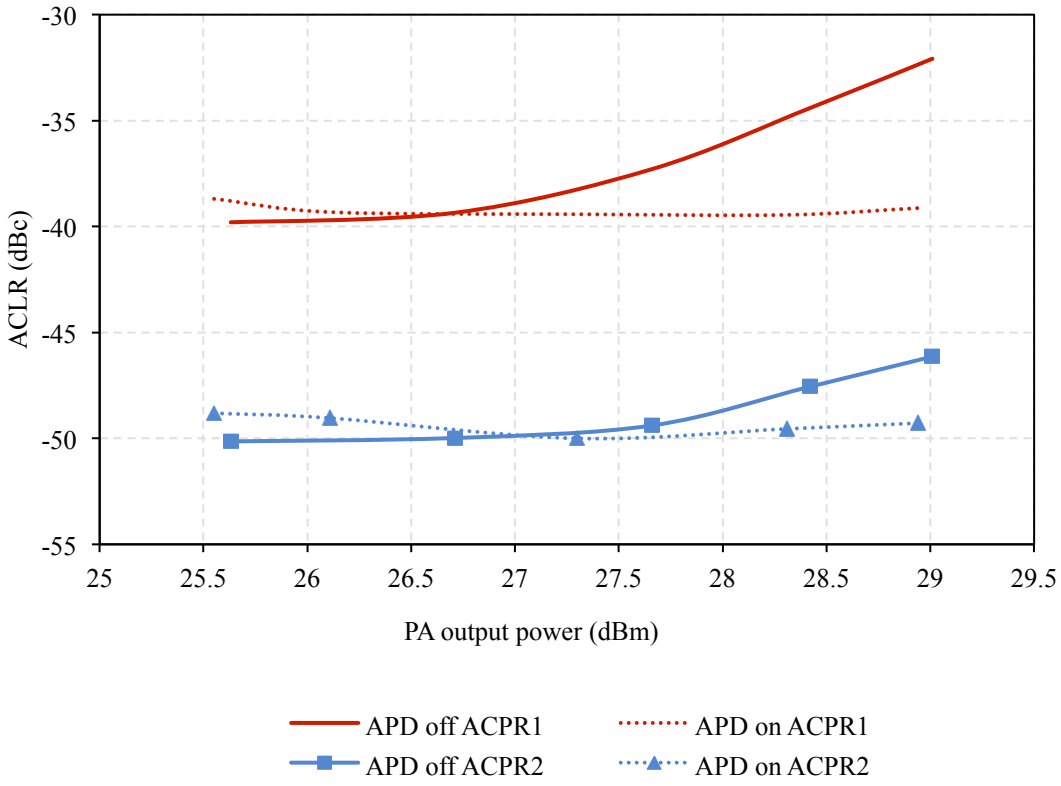
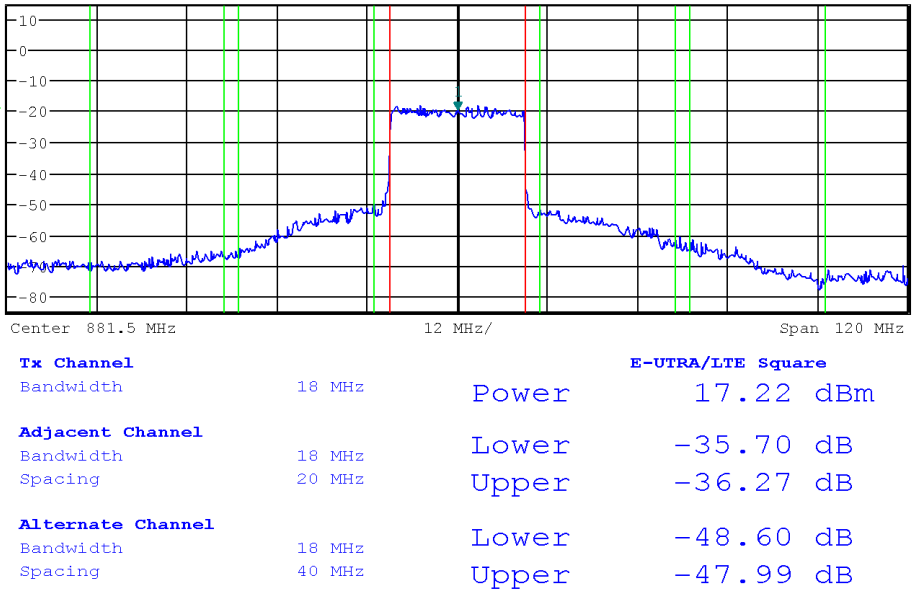
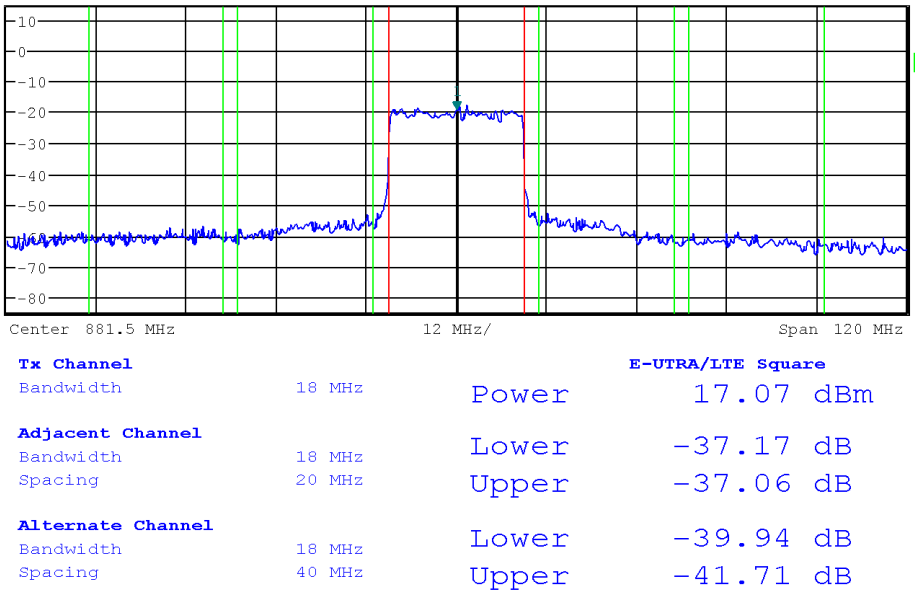



**Figure 5.18** Measured ACPR over PA output power (signal bandwidth =10 MHz)

Figure 5.18 shows the measured ACPR1 over different output power of Qorvo RFPA0875. This plot proves that this APD system is able to improve ACPR1 up to -40 dBc by compensating AM-AM and AM-PM errors in the PA. But achievable ACPR1 is limited by the noise caused by the gain block between the PA input and the output of the VPS and VGA die.




(a)




(b)

**Figure 5.19** PA output spectrum of the test board with an LTE 20 MHz signal input at output power of 28 dBm (a) APD off (b) APD on

An LTE 20 MHz signal with a 16QAM modulation was applied to the test board, and its output spectrums were observed at the output power of 27.5 dBm as shown in Figure 5.19. Figure 5.19 (a) is the output spectrum without the APD, and Figure 5.19 (b) is the

output spectrum with the APD. There was a 1 dB improvement in ACPR1, but ACPR2 got worse by 8 dB. As discussed in section 5.2.4, noise contributions from gain blocks appear severe, degrading APD performance when an LTE 20 MHz BW signal is applied.

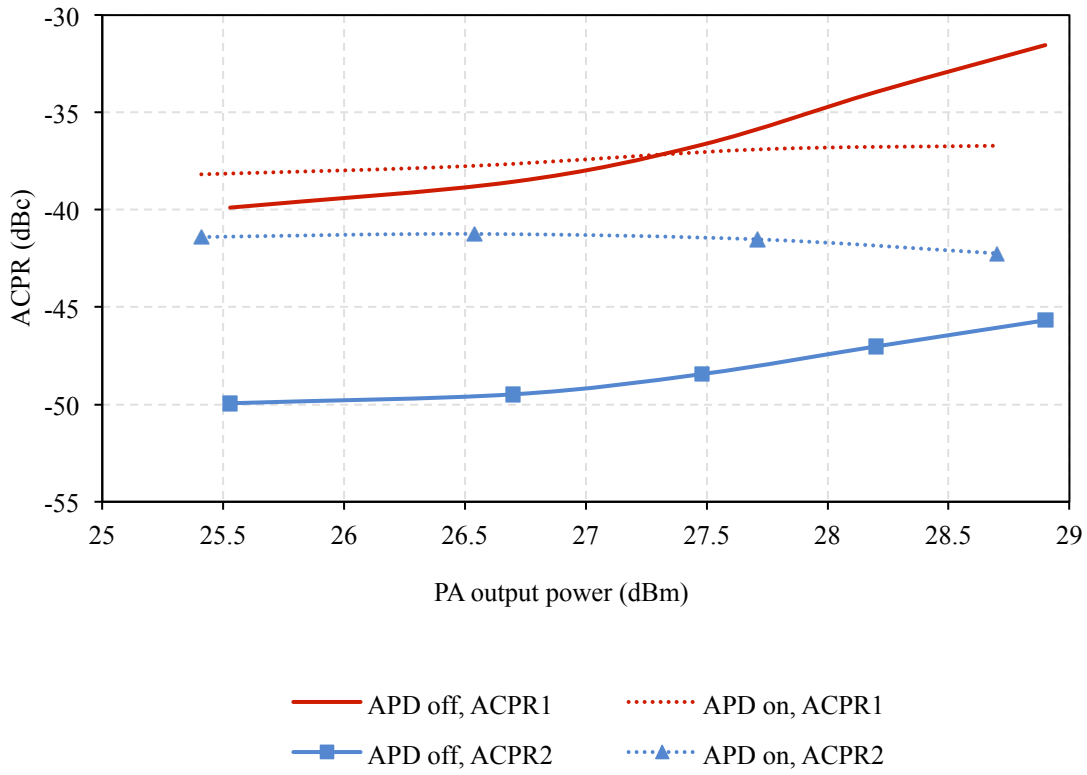



**Figure 5.20** Measured ACPR over PA output power (signal bandwidth =20 MHz)

Also, an LTE 5 MHz was applied to the test board, and the results are plotted in Figure 5.21. In this experiment, the 10 dB correction was measured at the output power of 28 dBm. As expected, achievable ACPR is better with an LTE 5 MHz signal than that with an LTE 10 MHz or 20 MHz. Since ACPR correction degrades as the channel BW of the input signal to the test board increases, it has been concluded that the main limitations of

the predistortion correction are noise generated by analog circuits and group delay in feedback circuits.

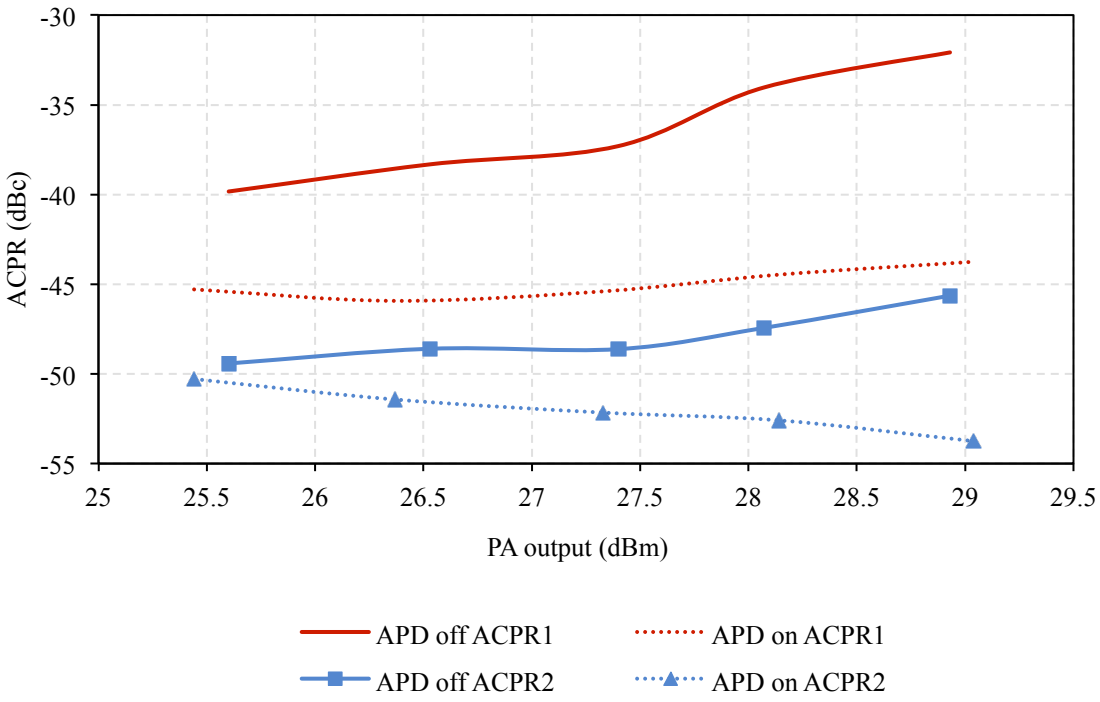



**Figure 5.21** Measured ACPR over PA output power (signal bandwidth =5 MHz)

When comparing above results with [21], this APD system was able to correct a signal having a wider BW, up to 10 MHz, for the 0.5 W PA at the output power of 28 dBm. Total power consumption of this test board was 437.66 mW, but half of the total power was dissipated at the gain blocks such as QPA4563 and SGA1263.

# CHAPTER 6

## CONCLUSIONS

In recent years, the demand for highly efficient and linear operation of an RF PA in a modern wireless transmitter has increased. DPD has been popular for a PA linearization, but DPD shows its limitations when the spectrum efficiency of modulated RF signals gets higher. As an alternative, APD is one of the most promising solutions because of its compact size, lower power consumption, and fewer complexities.

The research presented in this dissertation has been directed toward investigating ways to implement the predistortion of PA in the form of analog circuits or systems while providing the higher levels of performance required by 4G cellular systems. The achievements can be summarized as follows:

- Analog components for use in APD PA linearization systems, such as VPS, VGA, log amp, and phase detectors, are identified and analyzed to understand their behavior in the APD systems. Through excessive simulations in a Keysight (Agilent)'s Advanced Design System (ADS), the required specifications of each analog circuit are shown in this dissertation.
- Based on the specification requirements, VPS, VGA, and log amp are designed. First of all, the previously proposed VPS and VGA for use in APD applications have been analyzed by discussing their limitations that were not carefully considered. The VPS and the VGA not only fulfilled the required specifications but also were cascaded and integrated into a single die. This die is fabricated and verified

experimentally, which proves that this proposed die is suitable to use as an RF predistorter in APD applications.

- A log amp utilizing the digital calibration technique is proposed. The log amp consists of cascaded limiters and rectifiers. Each small-signal gain of limiters is adjusted by controlling the current DACs in tail transistors. These digital calibrating capabilities are used to compensate for the nonlinearities that might exist in the amplitude correction loop in APD systems. Furthermore, revised rectifiers that use the compound of PNP and NMOS are proposed to speed up the power detection in the log amp. This log amp is fabricated, and its measurements results obtained exceed conventional log amp performances in several areas, thus allowing its use in APD systems.
- An APD PA linearization system that uses the previously designed analog circuits such as VPS, VGA, and log amp is developed. To verify this system experimentally, its prototype board is fabricated, assembled, and tested. Digital calibrating capabilities are added to find the optimal operating condition of the APD systems by utilizing digitally calibratable log amps, DACs and digital potentiometers. The linearization performances for a 0.5 W GaAs pHEMP PA (Qorvo RFPA0875) were examined in the prototype board. It shows a 5 dB ACPR1 correction at an output power of 28 dBm, with an LTE 10 MHz signal, because of the accurate and fast analog circuits that are customized for this APD system. For an LTE 20 MHz signal, this APD system ends up with only a 1 dB ACPR1 correction because of the noise generated by analog circuits. The main limitations of the APD system come from the inherent loop delay in the systems and noise generated from each analog circuit.

# APPENDIX A

# DESIGN RESOURCES

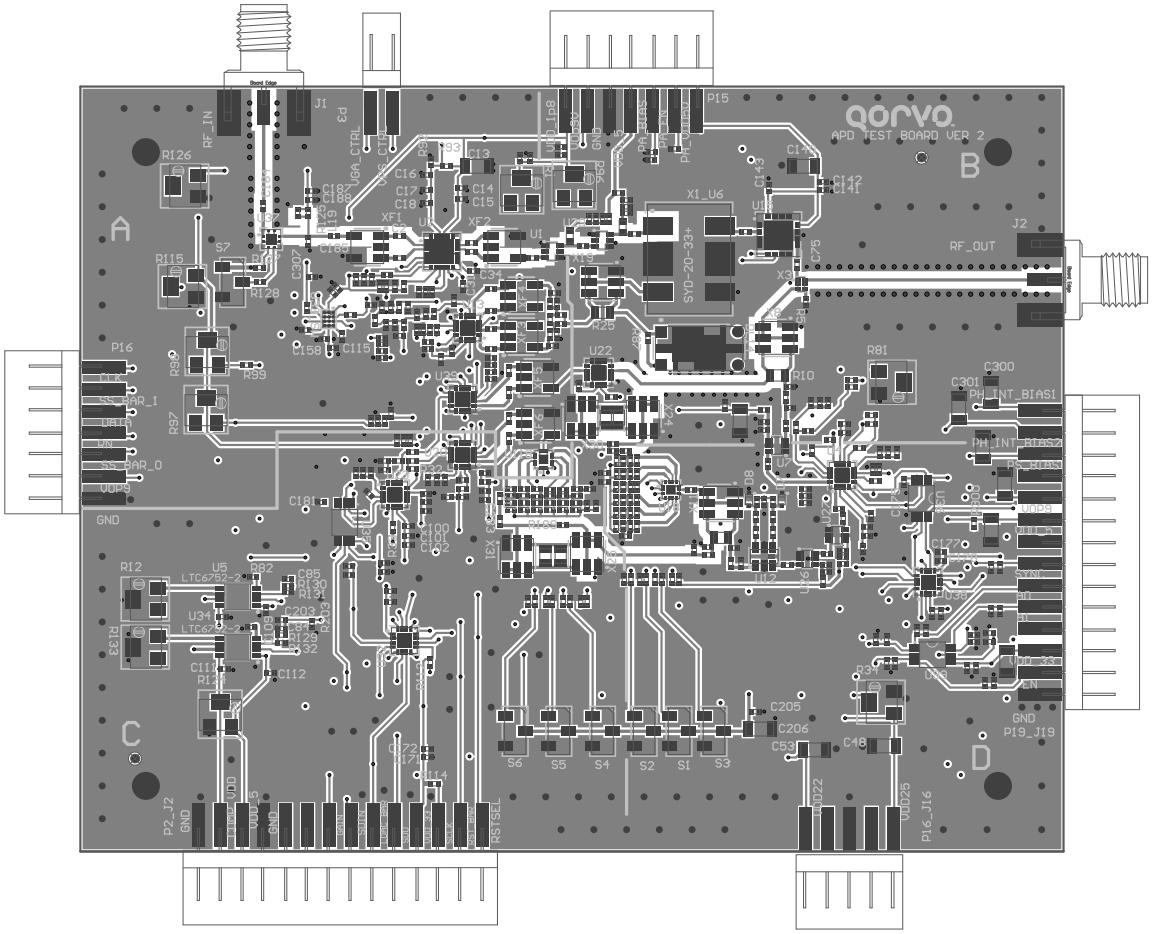



**Figure A.1** Layout of the analog predistortion test board

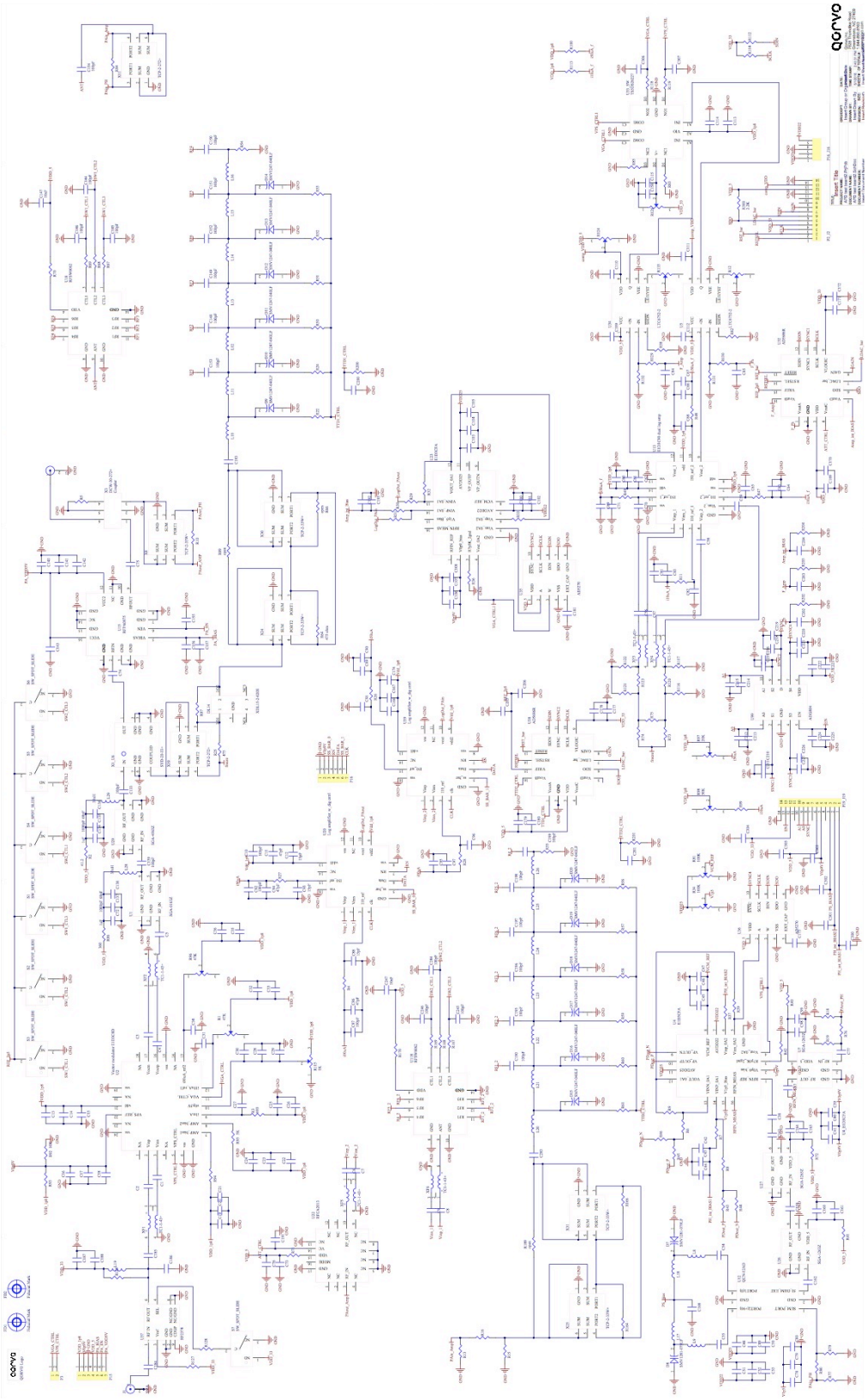


**Figure A.2** Schematic of the analog predistortion test board

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# VITA

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